

**M1535/M1535D/  
M1535+/M1535D+**

*(Super I/O with  
FIR Controller)  
Part 3 of 3*

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Note: Since April 2000, M1535/M1535D part 3 Datasheet has merged with M1535+/M1535D+ part 3 and will be referred to as the South Bridge in this manual.

**Section 1 : Super I/O with FIR Controller Register****1.1 Configuration Guide**

This configuration is based on the typical Plug-and-Play architecture and allows the BIOS to assign resources at POST. To assign the SOUTH BRIDGE a configuration key, <0x51, 0x23>, must be written to the CONFIG PORT to enter the CONFIGURE mode. Then follow the Plug-and-Play procedure to configure each device.

A configuration key = < 0xBB > must be written to the CONFIG PORT to exit the CONFIGURE mode and enter the NORMAL mode. After a hard reset or Power on reset, the SOUTH BRIDGE is in the NORMAL mode with all logical devices disabled except the KBC. The hardware setting pins control the KBC after the hard reset. The hardware settings are listed in the table below.

All logical devices may be configured through 2 standard Configuration I/O Ports (INDEX and DATA) by placing the SOUTH BRIDGE into Configuration Mode. The BIOS uses these configuration ports to initialize the logical devices during POST. The INDEX and DATA ports are only valid when the SOUTH BRIDGE is in Configuration Mode.

A hardware setting pin CFG\_PORT is latched to select the CFG\_PORT as 3F0h or 370h.

Port Name	CFG_PORT=1	CFG_PORT=0	Type
CONFIG PORT	0x3F0h	0x370h	W
INDEX PORT	0x3F0h	0x370h	W
DATA PORT	0x3F1h	0x371h	R/W

**Programming Example**

```
;-----  
; Enter Configuration mode,  
;-----  
MOV    DX,3F0H  
MOV    AX,051H  
CLI  
OUT    DX,AL  
MOV    AX,023H  
OUT    DX,AL  
  
;-----  
; Program register 0x60 of Logic Device 4  
;-----  
MOV    DX,3F0H  
MOV    AL,07H  
OUT    DX,AL    ; Point to Device Select Register  
MOV    DX,3F1H  
MOV    AL,04H  
OUT    DX,AL    ; Point to Device 4  
MOV    DX,3F0H  
MOV    AL,060H  
OUT    DX,AL    ; Point to Register 60H  
MOV    DX,3F1H  
MOV    AL,02H  
OUT    DX,AL    ; Update content of register 60H  
(repeat for other devices)  
;-----  
; Exit Configuration Mode  
;-----  
MOV    DX,3F0H  
MOV    AL,0BBH  
OUT    DX,AL
```

**Note :** The selected logic device number will keep its old value until the next new one is written.

## 1.2 Chip Level Registers

Index name Hard reset, Soft reset default values

Index 0x02h 0x00, 0x00

Bit	Description
7-1	Reserved
0	1 : Soft reset the configuration registers. This bit is automatically cleared after a write. This register is write only.

Index 0x07h 0x00, 0x00

Bit	Description
7-0	Select the current logical device. This allows the access to each logical device's registers.

Index 0x1Fh ALi defined device version.

Index 0x20h 0x53, 0x53  
ALi defined device identification. (read only)Index 0x21h 0x15, 0x15  
ALi defined device identification. (read only)

Index 0x22h 0x00, 0x00

Bit	Description
7	Read as 0.
6	Direct powerdown UART3 *0 0 : Disable 1 : Enable
5	Direct powerdown UART2 *0 0 : Disable 1 : Enable
4	Direct powerdown UART1 *0 0 : Disable 1 : Enable
3	Direct powerdown Parallel Port *0 0 : Disable 1 : Enable
2-1	Read as 0.
0	Direct powerdown FDC *0 0 : Disable 1 : Enable

\*0 - During direct powerdown, access to I/O ports are denied.  
To wake up the device, write a '0' to the corresponding bit.

Index 0x23h 0x00, 0x00

Bit	Description
7	Read as 0
6	Auto powerdown UART3. 0 : Disable 1 : Enable
5	Auto powerdown UART2. 0 : Disable 1 : Enable
4	Auto powerdown UART1. 0 : Disable 1 : Enable
3	Auto powerdown Parallel Port. 0 : Disable 1 : Enable
2-0	Read as 0.

Index 0x2Ch Reserved for test

Index 0x2Dh Reserved for test

Index 0x2Eh Reserved for test

**1.3 LOGICAL DEVICE 0 REGISTERS (FDC)****Index 0x30h** 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	FDC *1 0 : Disable 1 : Enable

\*1 - The disable function for this device has the same behavior as the direct powerdown function except that the device remains in the reset state.

**Index 0x60h** 0x03, 0x03

Bit	Description
7-0	The high address of the FDC's I/O base address.

**Index 0x61h** 0xF0, 0xF0

Bit	Description
7-3	The low address of the FDC's I/O base address.
2-0	Set to 0.

**Index 0x70h** 0x06, 0x06

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by FDC. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

**Index 0x74h** 0x02, 0x02

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by FDC. 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None

**Index 0xF0h** 0x08, 0x08

Bit	Description
7	0: Normal write protect signal 1: Force write protect signal
6-5	Read as 0
4	0 : No swap. 1 : Swap Drive 0 and Drive 1
3	0 : PS2 mode 1 : AT mode
2	Read as 0.
1	0 : Burst DMA mode. 1 : Non-burst DMA mode
0	Reserved

**Index 0xF1h** 0x00, 0x00

Bit	Description
7-4	Reserved
3-2	Density Select. 0x : Normal 10 : Force to 1 11 : Force to 0
1-0	External Floppy Select. 0x : Internal FDC 10 : External FDC 11 : Drive A internal, Drive B external

**Index 0xF2h** 0xFF, 0xFF

Bit	Description
7-0	Reserved

**Index 0xF4h** 0x00, 0x00

Bit	Description
7	Enable the PRT/FDD interface switch controlled by GPI29 0 : Disable this feature 1 : Enable this feature and the multi-function pin INTEJ/GPI29 in CFG_78_D1 of the SOUTH BRIDGE should be set to '1' for GPI29 selection. The PRT/FDD will switch to a printer interface if GPI29 is '1'. (Index 0xF1h bit 1 must be '0'.
6-5, 2	Read as 0.
3	Data Rate Table Select 0 : Regular drive 1 : 3-mode drive
1	0 : Normal 1 : Inverse DENSEL output
4, 0	Reserved.

**1.4 LOGICAL DEVICE 3 REGISTERS (Parallel Port)****Index 0x30h** 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	Activate Parallel Port. *1 0 : Disable 1 : Enable

\*1 - The disable function for this device has the same behavior as the direct powerdown function except that the device remains in the reset state.

**Index 0x60h** 0x03, 0x03

Bit	Description
7-0	The high address of the Parallel Port s I/O base address.

**Index 0x61h** 0x78, 0x78

Bit	Description
7-2	The low address of the Parallel Port s I/O base address.
1-0	Set to 0.

Note : An 8-byte boundary is required if EPP is enabled

**Index 0x70h** 0x05, 0x05

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by Parallel Port. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

**Index 0x74h** 0x04, 0x04

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by Parallel Port. 000 : DMA0 001 : DMA1 010 : DMA2 011 : DMA3 100 : None

**Index 0xF0h** 0x8C, 0x8C

Bit	Description
7	Parallel Port IRQ polarity 0 : Active high 1 : Active low
6-3	ECP FIFO threshold value. Default is 0001.
2-0	Parallel Port mode select 000 : PS2 001 : EPP 1.9 010 : ECP 011 : ECP+EPP1.9 100 : SPP (default) 101 : EPP 1.7 111 : ECP+EPP 1.7

**Index 0xF1h** 0xC5, 0xC5

Bit	Description
7-6	Output Pad type 00 : SPP – force driving PS2 – open drain EPP – open drain ECP – open drain 10 : SPP – open drain PS2 – force driving EPP – force driving EPP – force driving X1 : SPP – force driving PS2 –force driving EPP – force driving ECP - force driving
5-3	Read as 0.
2	Parallel Port operation clock 0 : 24MHz 1 : 12MHz
1	EPP time-out interrupt. 0 : Disable 1 : Enable
0	0 : Non-burst DMA mode. 1 : Burst DMA transfer mode in ECP.

**1.5 LOGICAL DEVICE 4 REGISTERS (UART1)****Index 0x30h** 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	UART1 *1 0 : Disable 1 : Enable

\*1 - The disable function for this device has the same behavior as the direct powerdown function except that the device remains in the reset state.

**Index 0x60h** 0x03, 0x03

Bit	Description
7-0	The high address of the UART1's I/O base address.

**Index 0x61h** 0xF8, 0xF8

Bit	Description
7-3	The low address of the UART1's I/O base address.
2-0	Set to 0.

**Index 0x70h** 0x04, 0x04

Bit	Description
7-4	Read as 0.
3-0	Select IRQ used by UART1. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

**Index 0xF0h** 0x00, 0x00

Bit	Description
7-3	Read as 0.
2	0 : Normal 1 : 8MHz clock source for UART1
1	High speed mode 0 : Disable 1 : Enable
0	MIDI support 0 : Disable 1 : Enable

**Index 0xF1h** 0x00, 0x00

Bit	Description
7-5	Read as 0.
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	0 : Full duplex in IR 1 : Half duplex in IR
1	IR transmit polarity. 0 : Active high 1 : Active low
0	IR receive polarity. 0 : Active high 1 : Active low

**Index 0xF2h** 0x0C, 0x0C

Bit	Description
7-6	Read as 0.
5	Timeout bit time definition. 0 : Bit time = baud rate 1 : Bit time = ( 1 / 115.2k ) = 8.68 us
4-3	IR half-duplex time-out time control. 00 : 41-bit time for Tx, 39-bit time for Rx. 01 : 42-bit time for Tx, 39-bit time for Rx. 1x : 40-bit time for Tx and Rx.
2	IR half-duplex Rx-to-Tx time-out timer. 0 : Disable 1 : Enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : Disable 1 : Enable
0	Baud Rate output on RI1. 0 : Disable 1 : Enable

## 1.6 LOGICAL DEVICE 5 REGISTERS (UART2)

Index 0x30h 0x00, 0x00

Bit	Description
7	FIR function 0 : Disable 1 : Enable
6-1	Read as 0.
0	UART2 *1 0 : Disable 1 : Enable

\*1 - The disable function for this device has the same behavior as the direct powerdown function except that the device remains in the reset state.

Index 0x60h 0x03, 0x03

Bit	Description
7-0	High address of the UART2' s I/O base address.

Index 0x61h 0xE8, 0xE8

Bit	Description
7-3	The low address of the UART2' s I/O base address.
2-0	Set to 0.

Index 0x70h 0x09, 0x09

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by UART2 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x74 0x04, 0x04

Bit	Description
7-3	Read as 0.
2-0	Select DMA channel used by FIR 000: DMA0 001: DMA1 010: DMA2 011: DMA3 100: None

Index 0xF0h 0x80, 0x80

Bit	Description
7,5	FIR transceiver module type 00: IBM-like module (TFDS-6000) 01: New HP-like module(HSDL 3600) 10: Old HP-like module(HSDL 1100) 11: Reserved.
6	FIR transceiver connector type 0: 5-pin (Vcc, IRRXH, IRRX2, Gnd, IRTX2) 1: 6-pin (Vcc, IRRXH, IRRX2, Gnd, IRTX2, CVROFF)
4	Status of FIR bank selection 0 : SIR bank 1 : FIR bank
3,1-0	Read as 0.
2	0 : Normal 1 : 8MHz clock source for UART2

Index 0xF1h 0x00, 0x00

Bit	Description
7-5	Read as 0.
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	1 : Half duplex in IR 0 : Full duplex in IR.
1	IR transmit polarity. 0: Active high 1: Active low
0	IR receive polarity. 0 : Active high 1 : Active low



**Index 0xF2h** 0x0Ch, 0x0Ch

Bit	Description
7-6	Read as 0.
5	Timeout bit time definition. 0 : Bit time = baud rate 1 : Bit time = (1/115.2k) = 8.68 us
4-3	IR half-duplex time-out time control. 1x : 40-bit time for Tx and RX 01 : 42-bit time for Tx, 39-bit time for Rx 00 : 41-bit time for Tx, 39-bit time for Rx
2	IR half-duplex Rx-to-Tx time-out timer 0 : Disable 1 : Enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : Disable 1 : Enable
0	Baud Rate output on IRRXH 0 : Disable 1 : Enable

Note: If UART2 enable bit=1 and FIR enable bit =1, then:  
(1) Change the registers from NS16550 to FIR. Continuously write bit 7-5 of base address +4 (Modem Control Register) as following values: 001,011,100,  
(2) Change registers from FIR to NS-16550, write one to bit 7 of base address +7 (FIR master block control register).

**1.7 LOGICAL DEVICE 7 REGISTERS (KEYBOARD)****Index 0x30h** N/A, 0x00h

Bit	Description
7-1	Read as 0.
0	Keyboard controller. This bit is initialized by hardware setting through RTS2J. 0 : Disable 1 : Enable

**Index 0x70h** 0x01h, 0x01h

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by Keyboard. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0x72h 0x00, 0x00

Bit	Description
7-4	Read as 0.
3-0	Select IRQ channel used by PS/2 Mouse. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

Index 0xF0h 0x00, 0x00

Bit	Description
7	Read as 0.
6	Read only. Indicates the type of keyboard. 0 : PS2. 1 : AT
5-4	Keyboard clock source speed. 00 : 8MHz 01 : 12MHz 10 : 16MHz 11 : Reserved
3-0	Read as 0.

## 1.8 LOGICAL DEVICE B REGISTERS (UART3)

Index 0x30h 0x00, 0x00

Bit	Description
7-1	Read as 0.
0	UART3 *1 0 : Disable 1 : Enable

\*1 - The disable function for this device has the same behavior as the direct powerdown function except that the device remains in the reset state.

Index 0x60h 0x02, 0x02

Bit	Description
7-0	The high address of the UART3's I/O base address.

Index 0x61h 0xF8, 0xF8

Bit	Description
7-3	The low address of the UART3's I/O base address.
2-0	Set to 0.

**Data Sheet**

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**Index 0x70h** 0x03, 0x03

Bit	Description
7-4	Read as 0.
3-0	Select IRQ used by UART3. 0000 : N/A 0001 : IRQ[1] 0010 : N/A 0011 : IRQ[3] 0100 : IRQ[4] 0101 : IRQ[5] 0110 : IRQ[6] 0111 : IRQ[7] 1000 : N/A 1001 : IRQ[9] 1010 : IRQ[10] 1011 : IRQ[11] 1100 : IRQ[12] 1101 : N/A 1110 : IRQ[14] 1111 : IRQ[15]

**Index 0xF0h** 0x00, 0x00

Bit	Description
7-3	Read as 0.
2	0 : Normal 1 : 8MHz clock source for UART3.
1	High speed mode 0 : Disable 1 : Enable
0	MIDI support 0 : Disable 1 : Enable

**Index 0xF1h** 0x00, 0x00

Bit	Description
7-5	Read as 0.
4-3	IR mode. 00 : Normal 01 : IrDA 10 : ASK IR 11 : Normal
2	0 : Full duplex in IR 1 : Half duplex in IR
1	IR transmit polarity. 0 : Active high 1 : Active low
0	IR receive polarity. 0 : Active high 1 : Active low

**Index 0xF2h** 0x0C, 0x0C

Bit	Description
7-6	Read as 0.
5	Timeout bit time definition. 0 : Bit time = baud rate 1 : Bit time = ( 1 / 115.2k ) = 8.68 us
4-3	IR half-duplex time-out time control. 00: 41-bit time for Tx, 39-bit time for Rx 01: 42-bit time for Tx, 39-bit time for Rx 1x: 40-bit time for Tx and Rx
2	IR half-duplex Rx-to-Tx time-out timer. 0 : Disable 1 : Enable
1	IR half-duplex Tx-to-Rx time-out timer. 0 : Disable 1 : Enable
0	Baud Rate output on RI2. 0 : Disable 1 : Enable

**1.9 LOGICAL DEVICE C REGISTERS (HOTKEY)****Index 0x30h** 0x00, 0x00

Bit	Description
7	Keyboard and mouse interface 1 : Swap keyboard and mouse interface 0 : Normal
6-2	Read as 0.
1	Mouse HOTKEY 0 : Disable 1 : Enable
0	Keyboard HOTKEY 0 : Disable 1 : Enable

**Index 0xF0h** 0x35, 0x35

Bit	Description
7-6	Read as 0.
5	Hotkey C is the last pressed key 0 : No 1 : Yes
4	Hotkey C 0 : Disable 1 : Enable
3	Hotkey B is the last pressed key 0 : No 1 : Yes
2	Hotkey B 0 : Disable 1 : Enable
1	Hotkey A is the last pressed key 0 : No 1 : Yes
0	Hotkey A 0 : Disable 1 : Enable

**Index 0xF1h** 0x14, 0x14 (Ctrl)

Bit	Description
7-0	Make code of Hotkey A

**Index 0xF2h** 0x11, 0x11 (Alt)

Bit	Description
7-0	Make code of Hotkey B

**Index 0xF3h** 0x71, 0x71 (Del)

Bit	Description
7-0	Make code of Hotkey C

**Index 0xF4h** Reserved.**Index 0xF5h** 0x05, 0x05

Bit	Description
7-4	Reserved.
3	Power saving mode (switching operation frequency) 0 : 8 MHz 1 : Full power on => 8 MHz Full power off => 1 MHz
2	Mouse HOTKEY control 0 : Single click 1 : Double click in 0.5 seconds
1	0 : Right Key disable 1 : Right Key enable
0	0 : Left Key disable 1 : Left Key enable

**Table 4-1 SOUTH BRIDGE Super I/O Hardware Setting Configuration**

Pin Name	Function
RTS1J	CFG_PORT
0	0x370h
1	0x3F0h
RTS2J	KBC_EN
0	Disable
1	Enable
DTR2J	PS2_ATJ (KBC)
0	AT mode
1	PS2 mode

**Table 4-2 Drive Mode bit mapping for DENSEL pin**

Data Rate	Bit 1-0 of 3F7h	Drive Mode bit of Index 0xF4	DENSEL
1Mbps	11	0	1
500Kbps	00	0	1
300Kbps	01	0	0
250Kbps	10	0	0
1Mbps	11	1	1
500Kbps	00	1	1
500Kbps	01	1	0
250Kbps	10	1	0

**1.10 Power Management Features**

The SOUTH BRIDGE contains power management features that makes it ideal for notebook and personal computer designs. These features are not recommended for ACPI compliant functions.

**1.10.1 Powerdown Modes of the FDC**

The FDC is powered down in two ways: direct powerdown and automatic powerdown. Direct powerdown results in immediate powerdown of the part regardless the current state of the part. Automatic powerdown is entered when certain conditions become true within the part.

**A. Direct Powerdown**

Direct powerdown is conducted via the POWER-DOWN bit in the DSR register (bit 6). Programming this bit high will powerdown the SOUTH BRIDGE after the part is internally reset. All current status is lost if this type of powerdown is used. The part can exit powerdown from this mode via any hardware or software reset. This type of powerdown will override the automatic powerdown. If the part is in automatic powerdown when the DSR powerdown is issued, then all the previous status of the part will be lost, and the SOUTH BRIDGE will be reset to its default values.

**B. Auto Powerdown**

Automatic powerdown is entered via a "Powerdown Mode" command. There are four conditions required before the part will enter powerdown. All these conditions must be true for the part to initiate the powerdown sequence. These conditions are listed as follows:

1. The motor enable pins MOT0 and MOT1 must be inactive,
2. The part must be idle; this is indicated by MSR = 80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupt),
3. The head unload timer must have expired, and
4. The auto powerdown timer must have timed out.

The command can be used to enable powerdown by setting the APD bit in the command to high. The command also provides a capability of programming a minimum power-up time via the DLY bit in the command. The minimum power-up time refers to a minimum amount of time the part will remain powered-up after being awakened or reset. An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down providing all the remaining conditions are met. Any software reset will re-initialize the timer.

Disabling the auto powerdown mode cancels the timers and will prevent the SOUTH BRIDGE from entering auto powerdown.

**1.10.2 WAKE UP MODES of FDC**

This section describes the conditions for awakening the FDC from both direct and automatic powerdown. Some amount of time is required for the FDC to exit the powerdown state and prepare the internal microcontroller to accept commands. Thus the recovery time of the wake-up process must be carefully controlled by the system software.

**A. Wake Up from DSR Powerdown**

If the SOUTH BRIDGE enters powerdown through the DSR powerdown bit, it must be reset to exit. Any form of software or hardware reset will reset the DSR's powerdown bit, although resetting the bit through the DSR is recommended. No other register access will awaken the part.

If the DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened by a software reset, the auto powerdown command (including the minimum delay timer) will again become effective as previously programmed. If the part is awakened via a hardware reset, the auto powerdown is disabled.

After reset, the part will go through a normal sequence. The drive status will be initialized. The FIFO mode will be set to default mode on a hardware reset or on a software reset if the LOCK command is not blocking it. Finally, after a delay, the polling interrupt will be issued.

**B. Wake Up from Auto Powerdown**

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by a reset or by appropriate access to certain registers.

If a hardware or software reset is used, then the part goes through the normal reset sequence. If the access is through the selected registers, then the SOUTH BRIDGE resumes operation as though it was never in powerdown. Besides activating the MR pin or one of the software reset bits in the DOR or DSR, the following register accesses will also wake-up the FDC:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not wake-up the part)
2. A read from the MSR register
3. A read or write to the FIFO register

Any of these actions will wake-up the FDC. Once awake, the SOUTH BRIDGE will initiate the auto powerdown time for 10 ms or 0.5 sec. (Depending on the DLY bit of the auto powerdown command). The part will powerdown again when all the powerdown conditions stated in the *Auto Powerdown* section are satisfied.

**1.10.3 Powerdown Mode of UART and Printer**

UART1, UART2 and the printer can enter auto powerdown by setting their relative powerdown bit in index 0x23.

**1.11 Floppy Disk Controller****1.11.1 Register Overview**

The FDC of the SOUTH BRIDGE is register and hardware-level compatible with the industry standard 765A and 82077SL standards. Table 1-1 below lists the I/O address map of the FDC controller.

**Table 1-1 FDC Controller I/O Address Map**

A2	A1	A0	R/W	Register
0	0	0	R	Status Register A, SRA
0	0	1	R	Status Register B, SRB
0	1	0	R/W	Digital Output Register DOR
0	1	1	R/W	Tape Drive Register TDR
1	0	0	R	Main Status Register MSR
1	0	0	W	Data Rate Select Register DSR
1	0	1	R/W	Data Register (FIFO)
1	1	0	X	Reserved
1	1	1	R	Digital Input Register DIR
1	1	1	W	Configuration Control Register CCR

**Status Register A (SRA), Read Only**

This is a read-only diagnostic register that is part of the PS/2 FDC register set, and is enabled when in the PS/2 mode. This register monitors the state of IRQ6 and some of the disk interface signals. The SRO can be read at any time when in PS/2 mode. In PC-AT mode, SD[7-0] are tri-state during a read.

Bit	Description
7	<b>Interrupt Pending</b> : The state of the Floppy Disk Interrupt output (active high).
6	<b>2nd Drive Installed</b> : Indicates if a second drive has been installed
5	<b>Step</b> : Active high status of the STEPJ pin
4	<b>Track 0</b> : Active low status of the TRK0J pin
3	<b>Head Select</b> : Active high status of the HDSELJ pin
2	<b>Index</b> : Active low status of the INDEXJ pin.
1	<b>Write Protect</b> : Active low status of the WPJ pin.
0	<b>Direction</b> : Active high status of the DIRJ pin.

**Status Register B (SRB), Read Only**

Bit	Description
7-6	<b>Reserved</b> : Always read as a logic "1".
5	<b>Drive Select 0</b> : Reflects the status of the Drive Select bit 0 of DOR (address 3F2, bit 0). This bit is cleared after a hardware reset. It is unaffected by a software reset.
4	<b>Write Data Toggle</b> : This bit changes state with every inactive edge of WDATAJ.
3	<b>Read Data Toggle</b> : Every inactive edge of RDATAJ causes this bit to change state.
2	<b>Write Gate</b> : Active high status of WGATEJ.
1	<b>Motor Enable 1</b> : The MOT1J disk interface output signal. This bit is low after a hardware reset and unaffected by a software reset.
0	<b>Motor Enable 0</b> : The MOT0J disk interface output signal. This bit is low after a hardware reset and unaffected by a software reset.

## Digital Output Register (R/W)

## Digital Output Register Description

Bit	Description
7	<b>Motor Enable 3:</b> This controls the Motor for drive 3, MOT3. The output is high when it is inactive, and low when it is active. This bit and DOR bit 6 provide information that controls the MOT1 and MOT0 pins, respectively when bit 7 of the configuration register is set.
6	<b>Motor Enable 2:</b> Same function as D7 except for drive 2's motor. Note that this signal is not brought out to a pin.
5	<b>Motor Enable 1:</b> This bit controls the Motor for drive 1's motor. When this bit is 0, the MOT1 output is high.
4	<b>Motor Enable 0:</b> Same as D5 except for drive 0's motor.
3	<b>DMA Enable:</b> When set to a 1, this enables the DRQ, DAK, and INT pins. A zero disables these signals.
2	<b>Reset Controller:</b> This bit resets the controller when 0 and enables normal operation when it is a 1. It does not affect the drive control or data rate registers which are reset only by a hardware reset.
1~0	<b>Drive Select:</b> These two pins are encoded for the four drive select, and are gated with the motor enable lines, so that only one drive is selected when its motor enable is active.

Table 1-2 Internal 4 Drive Decode - Normal

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DRV1	DRV0	MOT1	MOT0
x	x	x	1	0	0	1	0	/D5	/D4
x	x	1	x	0	1	0	1	/D5	/D4
x	1	x	x	1	0	1	1	/D5	/D4
1	x	x	x	1	1	1	1	/D5	/D4
0	0	0	0	x	x	1	1	/D5	/D4

Table 1-3 Internal 4 Drive Decode - Drives 0 and 1 Swapped

Digital Output Register						Drive Select Outputs		Motor on Outputs	
D7	D6	D5	D4	D1	D0	DRV1	DRV0	MOT1	MOT0
x	x	x	1	0	0	0	1	/D4	/D5
x	x	1	x	0	1	1	0	/D4	/D5
x	1	x	x	1	0	1	1	/D4	/D5
1	x	x	x	1	1	1	1	/D4	/D5
0	0	0	0	x	x	1	1	/D4	/D5



**Tape Drive Register (TDR)**

This register allows the user to assign tape support to a particular drive during initialization. A hardware reset sets all bits in this register to 0 making drive 0 not available for tape support. Drive 0 is reserved for the floppy boot drive.

Reg 3F3	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tapesel1	tapesel0

**Main Status Register**

The read-only main status register indicates the current status of the disk controller. It is always available to be read. One of its functions is to control the flow of data to and from the data register. It also indicates when the disk controller is ready to send or receive data. It should be read before each byte is transferred to or from the data register except during a DMA transfer. No delay is required when reading this register after a data transfer.

**Main Status Register Description**

Bit	Description
7	<b>Request for Master (RQM)</b> : Indicates that the data register is ready to send or receive data from the CPU. This bit is cleared immediately after a byte transfer, and is set again as soon as the disk controller is ready for the next byte.
6	<b>Data Direction (DIO)</b> : Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the data register.
5	<b>Non-DMA Execution</b> : This bit is set only during the execution phase of a command if it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the execution phase) must be monitored by the CPU either through interrupts, or software polling as described in the processor software interface section.
4	<b>Command in Progress</b> : This bit is set after the first byte of the command phase is written. This bit is cleared after the last byte of the result phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the command phase is written.
3~0	<b>Drives 3~0 Seeking</b> : This bit is set after the last byte of the command phase of a seek or recalibrate command is issued for drives 3~0, respectively. It is cleared after reading the first byte in the result phase of the sense interrupt command for this drive.

**Data Rate Select Register (DSR)****Datarate Select Register Description**

Bit	Description
7	<b>S/W RESET</b> behaves the same as DOR RESET except that this reset is self-clearing.
6	<b>POWERDOWN</b> bit implements direct powerdown. Setting this bit high puts the FDC into the powerdown state regardless of the state of the part. The part is reset internally and then put into powerdown. No status is saved and any operation in progress is aborted. Any hardware or software reset will exit the SOUTH BRIDGE from this powerdown state.
5	<b>Reserved</b> .
4~2	<b>PRECOMP 0-2</b> adjusts the WRDATA output to the disk to compensate for magnetic media phenomena known as bit shifting. The data patterns that are susceptible to bit shifting are well understood and the SOUTH BRIDGE compensates the data pattern as it is written to the disk. The amount of precompensation depends upon the drive and media but in most cases the default value is acceptable. The SOUTH BRIDGE starts precompensating the data pattern starting on Track 0. The CONFIGURE command can change the starting track for precompensation. The default value is selected if the three bits are zeros.
1~0	<b>DRATE 0-1</b> select one of the four data rates as listed in table on the next page. The default value is 250 Kbps upon a chip ("Hardware") reset. Other ("Software") Resets do not affect the DRATE or PRECOMP bits.

Table 1-4 Precompensation Delay Values Table

PRECOMP 432 bits	Precompensation Delay--DISABLED
111	0.00ns
001	41.67ns
010	83.34ns
011	125.00ns
100	166.67ns
101	208.33ns
110	250.00ns
000	DEFAULT

Table 1-5 Default Precompensation Delay Values

Data Rate	Precompensation Delay
1 Mbps	41.67ns
500 Kbps	125ns
300 Kbps	125ns
250 Kbps	125ns

Table 1-6 Data Rate

DRATESEL		Data Rate	
		MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

**Data Register (R/W)**

This is the location through which all commands, data, and status flow between the CPU and the FDC. During the command phase, the CPU loads the controller's commands into this register based on the status register request for master and data direction bits. The result phase transfers the status registers and header information to the CPU in the same fashion.

All command parameter information and disk data transfers go through the FIFO. The 16-byte FIFO has programmable threshold values. Data transfers are generated by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to a 765A compatible mode. The default values can be changed through the CONFIGURE command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk error. The table below gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold} \# * 1/\text{DATA RATE} * 8 - 1.5_{\mu\text{s}} = \text{DELAY}$$

Table 1-7 FIFO Service Delay Table

FIFO Threshold	Maximum Delay to Servicing
<b>Examples</b>	<b>at 1 Mbps Data Rate</b>
1 byte	$1 * 8_{\mu\text{s}} - 1.5_{\mu\text{s}} = 6.5_{\mu\text{s}}$
2 bytes	$2 * 8_{\mu\text{s}} - 1.5_{\mu\text{s}} = 14.5_{\mu\text{s}}$
8 bytes	$8 * 8_{\mu\text{s}} - 1.5_{\mu\text{s}} = 62.5_{\mu\text{s}}$
15 bytes	$15 * 8_{\mu\text{s}} - 1.5_{\mu\text{s}} = 118.5_{\mu\text{s}}$
<b>FIFO Threshold</b>	<b>Maximum Delay to Servicing</b>
<b>Examples</b>	<b>at 500 Mbps Data Rate</b>
1 byte	$1 * 16_{\mu\text{s}} - 1.5_{\mu\text{s}} = 14.5_{\mu\text{s}}$
2 bytes	$2 * 16_{\mu\text{s}} - 1.5_{\mu\text{s}} = 30.5_{\mu\text{s}}$
8 bytes	$8 * 16_{\mu\text{s}} - 1.5_{\mu\text{s}} = 126.5_{\mu\text{s}}$
15 bytes	$15 * 16_{\mu\text{s}} - 1.5_{\mu\text{s}} = 238.5_{\mu\text{s}}$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the SOUTH BRIDGE enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC.

**Configuration Control Register (CCR, PC-AT Modes)****Configuration Control Register Description**

Bit	Description
7~2	Not used.
1, 0	<b>Data Rate Select:</b> These bits set the data-rate and write-pre-compensation values for the disk controller. After a hardware reset, these bits are set to 1, 0 (250 Kbps).

**Digital Input Register (DIR, Read)****Digital Input Register Description (PC/AT mode)**

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the compliment of the value seen on the disk cable. The DSKCHG bit is forced inactive along with all the inputs from the floppy disk drive. All other bits remain tri-stated.
6~0	These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are in the high impedance state.

**Digital Input Register (PS/2 mode)**

Bit	Description
7	DSKCHG monitors the pin of the same name and reflects the compliment of the value seen on the disk cable.
6~3	undefined, always read as logic "1".
2~1	Data rate select. These bits control the data rate of the floppy controller. These bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.
0	High density. This bit is low whenever the 500 kbps or 1 Mbps data rates are selected, and high when 250 kbps and 300 kbps are selected.

## 1.11.2 Result Phase Status Registers

The result phase of a command contains bytes that hold status information. The format of these bytes are described in the following sections. Do not confuse these register bytes with the main status register which is a read-only register that is always available. The result phase status registers are read from the data register only during the result phase.

## Status Register 0 (ST0)

## Status Register 0 Description

Bit	Description
7~6	Interrupt Code : 00 = Normal termination of command. 01 = Abnormal termination of command. Command was executed, but not successfully completed. 10 = Invalid command issue. Command issued was not recognized as a valid command. 11 = Ready changed state during the polling mode.
5	Seek End: This bit is set after a seek or recalibrate command is completed by the controller. Used during sense interrupt commands.
4	Equipment Check: This bit is set after a recalibrate command track 0 signal failed to occur. Used during sense interrupt commands.
3	Not Used: 0
2	Head Number: At the end of the execution phase.
1, 0	Drive Select: At the end of the execution phase. 00 = Drive 0 selected      01 = Drive 1 selected 10 = Drive 2 selected      11 = Drive 3 selected

## Status Register 1 (ST1)

## Status Register 1 Description

Bit	Description
7	<b>End of Track:</b> This bit is set when the controller has transferred the last byte of the last sector without the TC pin becoming active. The last sector is the end-of-track sector number programmed in the command phase.
6, 3	<b>Not Used:</b> 0
5	<b>CRC Error:</b> If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the address field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the data field.
4	<b>Over Run:</b> This bit is set when the controller was not serviced by the CPU soon enough during a data transfer in the execution phase.
2	<b>No Data:</b> This bit is set for any three possible problems: 1. Controller cannot find the sector specified in the command phase during the execution of a read, write, or scan command. An address mark was found even if it is not a blank disk. 2. Controller cannot read any address fields without a CRC error during a read ID command. 3. Controller cannot find the starting sector during execution of a read track command.
1	<b>Not Writable:</b> Set if the write protect pin is active when a write or format command is issued.
0	<b>Missing Address Mark:</b> If this bit is set and bit 0 of ST2 is clear then the disk controller cannot detect any address field address mark after two disk revolutions. If bit 0 of ST2 is set, then the disk controller cannot detect the data field address mark.

**Status Register 2 (ST2)****Status Register 2 Description**

Bit	Description
7	<b>Not Used:</b> 0
6	<b>Control Mark :</b> This bit is set if the controller tried to read a sector which contained a deleted data address mark during execution of a read-data or scan command. Or, if a read-deleted-data command was executed, and a regular address mark was detected.
5	<b>CRC Error in Data Field:</b> This bit is set if the controller detected a CRC error in the data field. Bit 5 of ST1 is also set.
4	<b>Wrong Track:</b> This bit is set if the desired sector is not found, and the track number recorded on any sector of the current track is different from that stored in the track register.
3	<b>Scan Equal Hit:</b> This bit is set if the equal condition is satisfied during any scan command.
2	<b>Scan Not Satisfied:</b> This bit is set if the controller cannot find a sector on the track number recorded on any sector on the track which meets the desired condition during a scan command.
1	<b>Bad Track:</b> This bit is set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the track register and the recorded track number is FF.
0	<b>Missing Address Mark in Data Field:</b> This bit is set if the controller cannot find the data field address mark during a read/scan command. Bit 0 of ST1 is also set.

**Status Register 3 (ST3)****Status Register 3 Description**

Bit	Description
7	<b>Not Used:</b> 0
6	<b>Write Protect Status:</b> This bit is the complement of the associated FDC interface pin for the drive selected in DCR.
5	<b>Not Used:</b> 1
4	<b>Track 0 Status:</b> This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.
3	<b>Not Used:</b> 0
2	<b>Head Select Status:</b> This bit shows the status of the associated bit in the sense-drive-status command phase.
1, 0	<b>Drive Selected:</b> These bits show the status of the associated bits in the sense-drive-status command phase. These bits show the same status as ST0 bits 1, 0. 00 = Drive 0 selected      01 = Drive 1 selected 10 = Drive 2 selected      11 = Drive 3 selected

### **1.11.3 Controller Functional Description**

#### **Controller Phases**

The FDC handles commands in three phases —command, execution and result. Each phase is described below.

#### **Command Phase**

The CPU writes a series of bytes to the data register. These bytes indicate the command desired and the particular parameters required for the command. All bytes must be written in the order specified in the command description table. The execution phase starts immediately after the last byte in the command phase is written.

The Main Status Register controls the flow of command bytes, and must be polled by the software before writing each Command Phase byte to the Data Register. Prior to writing a command byte, bit 7 must be set and bit 6 must be cleared in the MSR. After the first command byte is written to the Data Register, bit 4 in the MSR is also set and remain set until the last Result Phase byte is read. If there is no Result Phase, it is cleared after the last command byte is written. A new command may be initiated after reading all the result bytes from the previous command.

#### **Execution Phase**

The disk controller performs the desired command. Some commands require the CPU to read or write data to or from the data register during this phase. Some commands such as Seek control the read/write head movement on the disk drive. Some commands do not involve any action by the uP or disk drive, and consists only of an internal operation by the controller.

If there is data to be transferred between the uP and the controller, there are three methods that can be used; DMA mode, interrupt mode, and software polling mode. All of these data transfer modes work with the FIFO enabled or disabled.

#### **DMA Mode**

If the DMA mode is selected, a DMA request is generated in the execution phase when each byte is ready to be transferred. To enable DMA operations during the execution phase, the DMA mode bit in the Specify command must be enabled, and the DMA signals must be enabled in the Drive Control Register. The DMA controller responds to the DMA request with a DMA-acknowledge and a read- or write-strobe. The DMA request is cleared by the active edge of the DMA-acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the result phase. TC is asserted to terminate an operation. Due to internal gating, TC is only recognized when the -DAK input is low.

#### **Interrupt Mode**

If the non-DMA mode is selected, an interrupt is generated in the execution phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register are set. The interrupt is cleared when the byte is transferred to or from the data register. The CPU should transfer the byte within the allotted time. If the byte is not transferred within the time allotted, an overrun error is indicated in the result phase when the command terminates at the end of the current sector.

An interrupt is also generated after the last byte is transferred. This indicates the beginning of the Result Phase.

#### **Software Polling**

If the non-DMA mode is selected and interrupts are not suitable, the CPU can poll the Main Status Register during the execution phase to determine when a byte is ready to be transferred. Bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the interrupt mode described above.

#### **Result Phase**

During the Result Phase, the uP reads a series of bytes from the data register. These bytes indicate the status of the command. This status may indicate whether the command executed properly, or may contain control information. Bits 7 and 6 in the MSR must both be set before each result byte can be read. After the last result byte is read, bit 4 in the MSR is cleared, and the controller is ready for the next command.

**Data Sheet****Command Set Descriptions**

Summary of the command set.

**Table 1-8 SOUTH BRIDGE FDC Command Table****READ DATA****Command Phase**

MT	MFM	SK	0	0	1	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data read from disk drive is transferred to system via DMA or Non-DMA modes.**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**READ DELETED DATA****Command Phase**

MT	MFM	SK	0	1	1	0	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data read from disk drive is transferred to system via DMA or Non-DMA modes.**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**READ A TRACK****Command Phase**

0	MFM	0	0	0	0	1	0
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data read from disk drive is transferred to system via DMA or Non-DMA modes.**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**READ ID****Command Phase**

0	MFM	0	0	1	0	1	0
0	0	0	0	0	HD	DR1	DR0

**Execution Phase:** Controller reads first ID Field header bytes it can find and reports these bytes to the system in the result bytes.**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**WRITE DATA****Command Phase**

MT	MFM	0	0	0	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**WRITE DELETED DATA****Command Phase**

MT	MFM	0	0	1	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data is transferred from the system to the controller via DMA or Non-DMA modes and written to the disk.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**FORMAT A TRACK****Command Phase**

0	MFM	0	0	1	1	0	1
0	0	0	0	0	HD	DR1	DR0
Bytes per Sector							
Sector per Track							
Format Gap							
Data Pattern							

**Execution Phase:** System transfers four ID bytes per sector to the floppy controller via DMA or Non-DMA modes. The entire track is formatted. The data block in the Data Field of each sector is filled with the data pattern byte.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Undefined
Undefined
Undefined
Undefined

**SCAN EQUAL****Command Phase**

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data transfer from the system to controller is compared to data read from disk.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector



**SCAN HIGH OR EQUAL****Command Phase**

MT	MFM	SK	1	1	1	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data transfer from the system to controller is compared to data read from disk

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**SCAN LOW OR EQUAL****Command Phase**

MT	MFM	SK	1	0	0	0	1
IPS	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data transfer from the system to controller is compared to data read from disk.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**VERIFY****Command Phase**

MT	MFM	SK	1	0	1	1	0
0	0	0	0	0	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Bytes per Sector							
End of Track Sector Number							
Intersector Gap Number							
Data Length							

**Execution Phase:** Data is read from the disk but not transferred to the system.

**Result Phase**

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes per Sector

**DUMPREG****Command Phase**

0	0	0	0	1	1	1	0
---	---	---	---	---	---	---	---

**Execution Phase:** Internal registers read

**Result Phase**

Present Track Number on Drive 0							
Present Track Number on Drive 1							
Present Track Number on Drive 2							
Present Track Number on Drive 3							
Step Rate Time				Motor Off Time			
Motor On Time							DMA
Sector per Track/End of Track							
LOCK	0	D3	D2	D1	D0	GAP	WG
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

**PERPENDICULAR MODE****Command Phase**

0	0	0	1	0	0	1	0
OW	0	D3	D2	D1	D0	GAP	WG

**Execution Phase:** Internal registers are written.

**No Result Phase.**

**CONFIGURE****Command Phase**

0	0	0	1	0	0	1	1
0	0	0	0	0	0	0	0
0	EIS	FIFO	POLL	FIFOTHR			
PRETRK							

**Execution Phase:** Internal registers are written.**No Result Phase****RECALIBRATE****Command Phase**

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

**Execution Phase:** Disk drive head is stepped out to Track 0.**No Result Phase****RELATIVE SEEK****Command Phase**

1	DIR	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
Relative Track Number							

**Execution Phase:** Disk drive head is stepped in or out a programmable number of tracks.**No Result Phase****SEEK****Command Phase**

0	0	0	0	1	1	1	1
0	0	0	0	0	HD	DR1	DR0
New Track Number							

**Execution Phase:** Disk drive head is stepped in or out to a desired track.**No Result Phase****SENSE DRIVE STATUS****Command Phase**

0	0	0	0	0	1	0	0
0	0	0	0	0	HD	DR1	DR0

**Execution Phase:** Disk drive status information is detected and reported.**Result Phase**

Status Register 3							
-------------------	--	--	--	--	--	--	--

**SENSE INTERRUPT****Command Phase**

0	0	0	0	1	0	0	0
---	---	---	---	---	---	---	---

**Execution Phase:** Status of interrupt is reported**Result Phase**

Status Register 0							
Present Track Number							

**SPECIFY****Command Phase**

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

**Execution Phase:** Internal registers are written.**No Result Phase****POWERDOWN MODE****Command Phase**

0	0	0	1	0	1	1	1
0	0	0	0	0	0	DLY	APD

**Execution Phase:** Internal registers are written**Result Phase**

0	0	0	0	0	0	DLY	APD
---	---	---	---	---	---	-----	-----

**VERSION****Command Phase**

0	0	0	1	0	0	0	0
---	---	---	---	---	---	---	---

**Result Phase**

1	0	0	1	0	0	0	0
---	---	---	---	---	---	---	---

**LOCK****Command Phase**

LOCK	0	0	1	0	1	0	0
------	---	---	---	---	---	---	---

**Execution Phase:** Internal registers are written.**Result Phase**

0	0	0	LOCK	0	0	0	0
---	---	---	------	---	---	---	---

**INVALID****Command Phase**

Invalid Codes							
---------------	--	--	--	--	--	--	--

**Result Phase**

Status Register 0 (80H)							
-------------------------	--	--	--	--	--	--	--

**1.11.4 Command Description****Read Data**

The read data op-code is written to the data register followed by 8 bytes as specified in the command table. After the last byte is written, the controller starts looking for the correct sector header. Once the controller is found, the controller sends data to the CPU. After one sector is finished, the sector number is incremented by one and this new sector is searched for. If MT (multi-track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by the end of track sector number is reached. Then, side one is read by starting with sector number one.

In DMA mode, the read-data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC should be controlled by the CPU and be asserted when enough bytes are received. An alternative to these methods of stopping the read-data command is to program the end of track sector number as the last sector number to be read. The controller stops reading the disk with an error message indicating that it tried to access a sector number beyond the end of the track.

The number of data bytes per sector parameter is defined in the table below. If this is set to zero, the data length parameter defines the number of bytes that the controller transfers to the CPU. If the data length specified is smaller than 128, the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the data length parameter are transferred to the CPU. Data length parameter should not be set to zero. If the number of bytes per sector parameter is not zero, the data length parameter has no meaning and should be set to FFh.

**Table 1-9 Sector Size Selection**

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

If the implied seek mode is enabled by both the CONFIGURE command and the IPS bit in this command, a seek is performed to the track number specified in the command phase. The controller also waits for the head-settle-time if the implied seek is enabled. After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number of bytes/sector given in the command phase with the appropriate bytes read off the disk in the address fields.

If the correct sector is found, but there is a CRC error in the address field, bit 5 of ST1 (CRC error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (no data) is set and an abnormal termination is indicated. In addition to this, if any address field track number is FFh, bit 1 of ST2 (bad track) is set or, if any address field track number is different from that specified in the command phase, bit 4 of ST2 (wrong track) is set.

After finding the correct sector, the controller reads that data field. If a deleted data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the data field, bit 5 is set in both ST1 and ST2 (CRC error) and an abnormal termination is indicated.

If no problems occur in the read command, the read continues from one sector to the next in logical order (not physical order) until either TC is set or an error occurs. If a disk has not been inserted into the drive, there are many opportunities for the controller to hang. It does this if it is waiting for a certain number of disk revolutions. If this occurs, the controller can be forced to abort the command by writing a byte to the data register.

An interrupt is generated when an execution phase of the read data command terminates. The following table shows the values that are read back in the result phase. If an error occurs, the result bytes indicate the sector being read when the error occurred.

Table 1-10 Result Phase Termination Values with No Error Table

Last	ID Information at Result Phase					
MT	HD	Sector	Track	Head	Sector	B/S
0	0	< EOT	NC	NC	S + 1	NC
0	0	= EOT	T + 1	NC	1	NC
0	1	< EOT	NC	NC	S + 1	NC
0	1	= EOT	T + 1	NC	1	NC
1	0	< EOT	NC	NC	S + 1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S + 1	NC
1	1	= EOT	T + 1	0	1	NC

EOT = End of track sector number from command phase

S = Sector number last operated on by controller

NC = No change in value

T = Track number programmed in command phase

**Read-Deleted-Data**

This command is the same as the read-data command except for how it handles a deleted data mark. If a deleted data mark is read, the sector is read normally. If a regular data mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (control mark) is set, and the next sector is searched for. If a regular data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (control mark) is set, and the read terminates with a normal termination.

**Write-Data**

The write-data command is very similar to the read-data command except that data is transferred from the CPU to the disk rather than the other way around. If the controller detects the write-protect signal, bit 1 of ST1 (not writable) is set and an abnormal termination is indicated.

**Write-Deleted-Data**

This command is the same as the write-data command except that a deleted-data mark is written at the beginning of the data field instead of the normal data mark.

**Read a Track**

This command is similar to the read-data command except for the following: the controller starts at the index hole and reads the sectors in their physical order, not their logical order. Even though the controller reads sectors in their physical order, it still compares the header ID bytes with the data programmed in the command phase. The exception to this is the sector number. Internally, this is set to one, then incremented for each successive sector read. Whether or not the programmed address field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No data) is set, but the operation continues. If there is a CRC error in the address or data field, the read also continues. The command terminates when it has read the number of sectors programmed in the EOT parameter.

**Read ID**

This command causes the controller to read the first address field it finds. The result phase contains the header bytes that are read. There is no data transfer during the execution phase of this command. An interrupt is generated when the execution phase is completed.

**Format-a-Track**

This command formats one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, address fields, and data fields. The exact details of the number of bytes for each field is controlled by the parameters given in the format-a-track command. The data field consists of the fill-byte specified in the command, repeated to fill the entire sector. To allow for floppy formatting, the CPU must supply the four address field bytes (track, head, sector, number of bytes) for each sector formatted during the execution phase. In other words, as the controller formats each sector, it requests four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. The following tables show some typical values for the programmable gap size.

The format command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the result phase are significant.

Table 1-11 Gap Length for Various Sector Sizes and Disk Types Table

Mode	Sector Size (Dec)	Sector Code (Dec)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
<b>8-inch Drives (360 RPM, 500 kb/s)</b>					
FM	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
MFM	4096	05	01	C8	FF
	256	01	0F	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
<b>5.25-inch Drives (300 RPM, 250 kb/s)</b>					
FM	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
MFM	2048	04	01	C8	FF
	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
<b>3.5-inch Drives (300 RPM, 250 kb/s)</b>					
FM	128	00	0F	07	1B
	256	01	09	0E	2A
	512	02	05	1B	3A
MFM	256	01	0F	0E	36
	512	02	09	1B	54
	1024	03	05	35	74

Table 1-12 Format Table for PC-Compatible Diskette Media Table

Media Type	Sector Size (Dec)	Sector Code (Hex)	EOT (Hex)	Sector Gap (Hex)	Format* Gap (Hex)
360 K	512	02	09	2A	50
1.2 M	512	02	0F	1B	54
720 M	512	02	09	1B	50
1.44 M	512	02	12	1B	6C
2.88 M	512	02	24	1b	54

\* Format gap is the gap length used only for the format command.

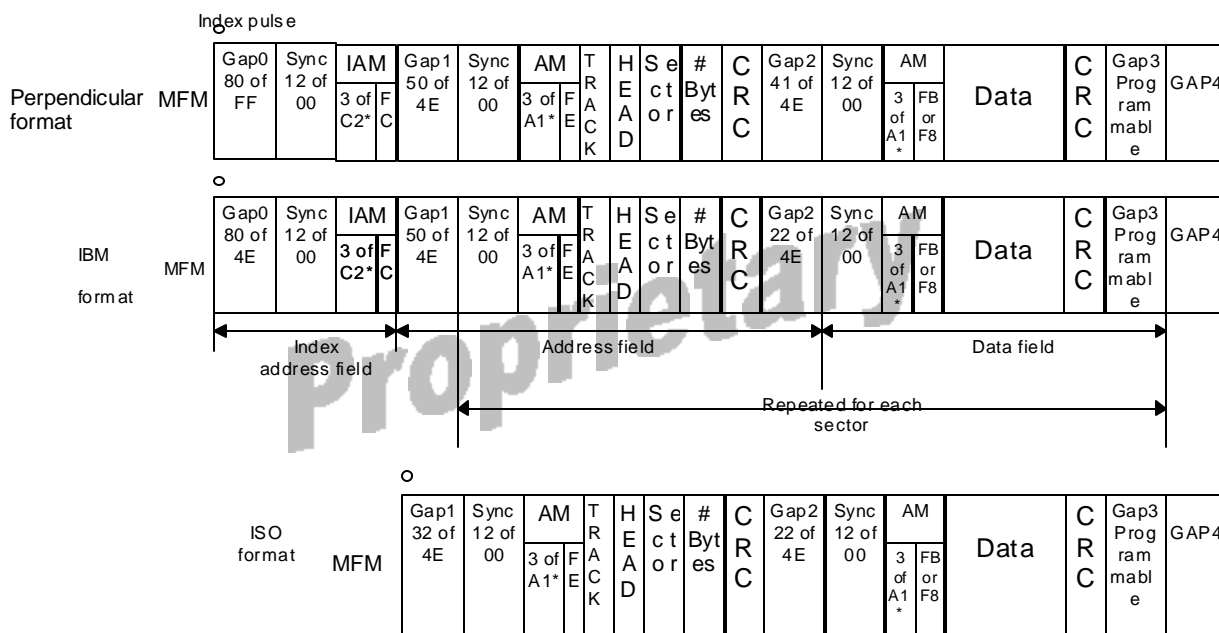


Figure 1-1 IBM, Perpendicular, and ISO Formats Supported by the Format Command

### Scan Commands

The scan commands allow data read from the disk to be compared against data sent from the CPU. There are three scan commands to choose from:

Scan equal	Disk data = CPU data
Scan less than or equal	Disk data ≤ CPU data
Scan greater than or equal	Disk data ≥ CPU data

Each sector is interpreted with the most significant byte first. If the wildcard mode is enabled from the mode command, an FFh from either the disk or CPU is used as a "don't care" byte that always matches equal. If each sector is read, the desired condition has not been met, and the next sector is read. The next sector is defined as the current sector number plus the sector step-size specified.

The scan command continues until the scan condition has been met, or the end of track sector number has been reached, or if TC is asserted. If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command terminates with D3 of ST2 set (scan equal hit). Table 1-13 shows the result phase of the command.

Table 1-13 Scan Command Termination Values

Status Register Command	D2	D3	Conditions
Scan equal	0	1	Disk = CPU
	1	0	Disk <> CPU
Scan low or equal	0	1	Disk = CPU
	0	0	Disk < CPU
	1	0	Disk > CPU
Scan high or equal	0	1	Disk = CPU
	0	0	Disk < CPU
	1	0	Disk > CPU

### Seek

There are two ways to move the disk drive head to the desired track number. The first method is to enable the implied seek mode. This way, each individual read or write command automatically moves the head to the track specified in the command.

The second method is by using the seek command. During the execution phase of the seek command, the track number to seek for is compared with the present track number, and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the specify command until the head reaches the correct track. At this point, an interrupt is generated and a sense-interrupt command is required to clear the interrupt.

During the execution phase of the seek command, the only indication via software that a seek command is in progress is bits 0~3 (drive busy) of the main status register. Bit 4 of the main status register (command in progress) is not set. While the internal micro-engine is capable of multiple seeks on two or more drives at the same time since the drives are selected via the drive-control register in software, software should ensure that only one drive performs the seek command at one time. No other command except the sense-interrupt command is issued while a seek command is in progress.

#### Relative Seek

The Relative Seek command steps the selected drive in or out a given number of steps. This command will step the read/write head an incremental number of tracks from the current track number, contrasting to step it to the desired track number as Seek command. The Relative Seek parameters are defined as follows:

**DIR:** Read/Write Head Step Direction Control  
0=Step Head Out, 1=Step Head In

**RTN:** Relative Track Number. This value will determine how many incremental tracks to step the head in or out from the current track number.

#### Recalibrate

The recalibrate command is very similar to the seek command. It is used to step a drive head out to track zero. Step pulses are produced until the track zero signal from the drive becomes true. If the track zero signal does not go true before 80 step pulses are issued, an error is generated.

Recalibrations on more than one drive at a time should not be issued for the same reason as explained in the seek command. No other command except the sense-interrupt command should be issued while a recalibrate command is in progress.

#### Sense-Interrupt Status

An interrupt is generated by the controller when any of the following conditions occur:

1. Upon entering the result phase of:
  - a. Read-data command
  - b. Read-deleted-data command
  - c. Write-data command
  - d. Write-deleted-data command
  - e. Read-a-track command
  - f. Read-ID command
  - g. Format command
  - h. Scan commands
2. During data transfers in the execution phase while in the non-DMA mode
3. Internal ready signal changes state (only occurs immediately after a hardware or software reset).
4. Seek or recalibrate command termination

An interrupt generated for reasons 1 and 2 above occurs during normal command operations and are easily recognized by the CPU. During an execution phase in non-DMA mode, bit 5 (execution mode) in the MSR is set to 1. Upon entering result phase, this bit is set to 0.

Reasons 1 and 2 do not require the sense interrupt status command. The interrupt is cleared by reading or writing information to the data register. Interrupts caused by reasons 3 and 4 are identified with the aid of the sense interrupt status command. This command resets the interrupt when the command byte is written.

Following table shows how to identify the cause of the interrupt by using bits 5, 6 and 7 of ST0.

Issuing a sense-interrupt status command without an interrupt pending is treated as an invalid command. If the extended track range mode is enabled, a third byte should be read in the result phase which indicates the four most significant bits of the present track number. Otherwise, only two bytes should be read.

**Specify**

The specify command sets the initial values for each of the three internal timers. The table below shows the timer programming values.

The head-load and head-unload timers are artifacts of the UPD765A. These timers determine the delay from loading the head until a read or write command is started, and unloading the head sometime after the command was completed.

The step-rate time defines the time interval between adjacent step pulses during a seek, implied-seek, or recalibrate command. The times stated in Table 1-15 are affected by the data rate. These values are for 500 kb/s MFM (250 Kb/s FM) and 1 Mb/s MFM (500 Kb/s FM). For 300 kb/s MFM data rate (150 Kb/s FM), these values, multiply by 1.6667, and for 250 Kb/s MFM (125 Kb/s FM) double these values.

The choice of DMA or non-DMA operation is made by the non-DMA bit. When this bit is 1, the non-DMA mode is selected, and when this bit is 0, DMA mode is selected. This command does not generate an interrupt.

**Table 1-14 Status Register 0 Termination Codes**

Interrupt Code D7	D6	D5	Seek End Cause
1	1	0	Internal ready went true
0	0	1	Normal seek termination
0	1	1	Abnormal seek termination

**Table 1-15 Step, Head, Load and Unload Timer Definitions (500 kb/s MFM)**

Timer	Mode 1 Value	Range	Mode 2 Value	Range	Unit
Step Rate	(16 - N)	1~16	(16 - N)	1~16	ms
Head Unload	N x 16	0~240	N x 512	0~7680	ms
Head Load	N x 2	0~254	N x 32	0~4064	ms

**Sense Drive Status**

This two-byte command obtains the status of a disk drive. Status register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

**Verify**

The VERIFY command is used to verify the data stored on a disk. This command acts exactly like a READ DATA command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously stored value.

**Version**

The Version command can be used to determine the floppy controller being used. The result phase uniquely identifies the floppy controller version. The FDC returns a value of 90h in order to be compatible with the 82077. For older versions compatible with the NEC765 controller, a value of 80h (invalid command) will be returned.

**Dumpreg**

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. The command returns important information regarding the status of many of the programmed field in the FDC. This can be used to verify the values initialized in the FDC.

**Configure**

The Configure command controls some operation modes of the controller. It should be issued during the initialization of the FDC after power up. These bits are set to their default values after a hardware reset.

**EIS:** Enable implied seek. When EIS=1, the FDC will perform a SEEK operation before executing a read/write command. The default value is 0 (no implied seek).

**EFIFO:** Enable FIFO. When EFIFO=1, the FIFO is disabled (NEC765A compatible mode). This means data is transferred on a byte by byte basis. The default value is 1 (FIFO disable).

**POLL:** Disable Polling. When POLL=1, polling of the drives is disabled. POLL defaults to 0 (polling enable). When enabled, a single interrupt is generated after reset.

**FIFOTHR:** The FIFO threshold in the execution phase of a read/write command. This is programmable from 1 to 16 bytes. FIFOTHR defaults to 00. A 00h selects one byte and 0Fh selects 16 bytes.

**PRETRK:** Precompensation start track number. Programmable from track 0 to 255. PRETRK defaults to track 0. A 00h selects track 0 and a FFh selects track 255.



**Powerdown Mode**

The Powerdown mode command allows for automatic power management. The use of this command can extend the battery life in portable PC applications. To enable auto powerdown, the command may be issued during the BIOS power on self test (POST).

**DLY:** Minimum power-up timer. This bit is active only if the APD bit is enabled. Setting this bit to 0 assigns a 10msec timer, and to 1, assigns a 0.5sec timer. The timer will be re-initialized after a command execution is finished (idle state) and start to countdown. When the timer is expired, the FDC will enter the powerdown state automatically.

**APD:** Enable auto powerdown. When set to 1, the auto powerdown is enabled.

**Lock**

The Lock command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the EFIFO, FIFOTHR and PRETRK bits in the Configure command are not affected by a software reset.

After the command byte is written, the result byte must be read before continuing to the next command.

**Invalid**

If an invalid command (illegal Opcode byte in the command phase) is received by the controller, the controller responds with ST0 in the Result Phase. The controller does not generate an interrupt during this condition. The system reads an 80h from ST0 indicating an invalid command was received.

**Perpendicular Mode**

The Perpendicular Mode command is designed to support the Perpendicular Recording disk drives (4Mbytes unformatted capacity). The Perpendicular Mode command configures each of the four logical drives as a perpendicular or conventional disk drive. Configuration of the four logical disk drives is done via the D3-D0 bits, or with the GAP and WG control bits. This command should be issued during the initialization of the floppy controller.

A 0 written to Dn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW bit offers additional control. When OW=1, changing the values of D3-D0 is enabled. When OW=0, the internal values of D3-D0 are unaffected, regardless of what is written to D3-D0.

The function of the Dn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are not set to 00, they overrides whatever is programmed in the Dn bits. The table below indicates the operation of the FDC based on the values of GAP and WG. D3-D0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset resets all of these bits to zero.

**Table 1-16 Effects of WG and GAP bits Table**

GAP	WG	Mode	GAP2 Length during Format	Portion of GAP2 re-written by Write Data Command
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1Mbps)	41 Bytes	38 Bytes

### 1.11.5 Parallel Port Mode FDC

In this mode, the floppy disk control signals are available on the parallel port pins. When this mode is selected, the parallel port is not available. There are four modes of operation. These modes can be selected in index 0xF1h of the FDC configuration space. The FDC signals are multiplexed onto the Parallel port pins as shown in table below.

0xF1[1:0]		Parallel port function
0	0	printer
0	1	printer
1	0	FDC (drive 0 or 1)
1	1	FDC (drive 1)

Conn Pin no.	SPP mode	Type	FDC mode	Type
1	STROBJ	I/O	DRV0	O
2	PD[0]	I/O	INDEXJ	I
3	PD[1]	I/O	TRK0J	I
4	PD[2]	I/O	WPJ	I
5	PD[3]	I/O	RDATAJ	I
6	PD[4]	I/O	DSKCHGJ	I
7	PD[5]	I/O		
8	PD[6]	I/O	MOT0	O
9	PD[7]	I/O		
10	ACKJ	I	DRV1	O
11	BUSY	I	MOT1	O
12	PE	I	WDATAJ	O
13	SLCT	I	WGATEJ	O
14	AUTOFDJ	I/O	DENSEL	O
15	ERRORJ	I	HDSELJ	O
16	INITJ	I/O	DIRJ	O
17	SLCTINJ	I/O	STEPJ	O

### 1.12 Serial Port Registers

Each of the serial ports function as data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a tri-state 8-bit bi-directional data bus.

The UARTs are completely independent and perform serial-to-parallel conversion on data characters received from a peripheral device or a modem, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of any of the UARTs at any time during the functional operation. Status information reported includes the type and condition of the transfer

operations performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt). The UARTs have programmable baud rate generator capable of dividing the timing reference clock input by divisors of 1 to ( $2^{16} - 1$ ), and producing a 16 X clock for driving the internal transmitter logic. Provisions are also included to use this 16X clock to drive the receiver logic. The UARTs have complete modem-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle communications link.

The following table 1-17 lists the register addresses A2 ~ A0 (AEN is equal to zero). DLAB is the divisor latch access bit.

**Table 1-17 Serial Port Registers Table**

Register Address	Access (AEN=0)	Abbreviation	Register Name	Access
Base +	DLAB			
0h	0	THR	Transmit Holding Register	W
0h	0	RBR	Receiver Buffer Register	R
0h	1	DLL	Divisor Latch LSB	R/W
1h	1	DLM	Divisor Latch MSB	R/W
1h	0	IER	Interrupt Enable Register	R/W
2h	-	IIR	Interrupt Identification Register	R
2h	-	FCR	FIFO Control Register	W
3h	-	LCR	Line Control Register	R/W
4h	-	MCR	Modem Control Register	R/W
5h	-	LSR	Line Status Register	R
6h	-	MSR	Modem Status Register	R
7h	-	SCR	Scratch Pad Register	R/W

Table 1-18 Register Summary for each UART Channel Table

			Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	Receiver Buffer Register (Read only)	R B R	Data bit 0 (Note 1)	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
0	Transmitter Holding Register (Write only)	T H R	Data bit 0	Data bit 1	Data bit 2	Data bit 3	Data bit 4	Data bit 5	Data bit 6	Data bit 7
1	Interrupt Enable Register	I E R	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Enable Receiver Line Status Interrupt (ELSI)	Enable Modem Status Interrupt (EMSI)	0	0	0	0
2	Interrupt Ident. Register (Read only)	I R	0 if interrupt pending	Interrupt ID bit	Interrupt ID bit	0	0	0	FIFO enable	FIFO enable
2	FIFO control register (write only)	F C R	FIFO enable	RCVR FIFO Reset	Xmit FIFO reset	reserved	reserved	Reserved	RCVR Trigger (LSB)	RCVR Trigger (MSB)
3	Line control register	L C R	Word Length Select bit 0 (WLS0)	Word Length Select bit 1 (WLS1)	Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
4	Modem control register	M C R	Data Terminal ready (DTR)	Request to send (RTS)	Out 1 (Note 2)	IRQ Enable (Note 2)	Loop	0	0	0
5	Line status register	L S R	Data ready (DR)	Overrun error (OE)	Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register Empty (THRE)	Transmitter Empty (TEMT)	Error in RCVR FIFO
6	Modem status register	M S R	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)	Trailing Edge ring indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
7	Scratch register (Note 4)	S C R	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 DLA B=1	Divisor latch (LS)	D L L	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 DLA B=1	Divisor latch (MS)	D L M	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

- Note
1. Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
  2. This bit no longer has a pin associated with it.

**Line Control Register (LCR)**

The system programmer uses this read/write register to specify the format of the asynchronous data communications exchange and set the divisor latch access bit.

**LCR Registers**

Bit	Description
7	Divisor latch access bit (DLAB). 1 = To access divisor latches of the baud generator. 0 = To access other registers.
6	Break control bit. This bit causes a break condition to be transmitted to the receiving UART. 1 = Serial output (SOUT) is forced to the spacing logic (logic 0) 0 = Break is disabled This bit acts only on SOUT and has no effect on transmitter logic. This enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters are transmitted because of the break: 1. Load all 0s, pad character in response to THRE. 2. Set break after the next THRE. 3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored. During the break, the transmitter can be used as a character timer to accurately establish the break duration.
5	Stick parity bit. When parity is enabled, it is used in conjunction with bit 4 to select, mark or space parity. 1 = Enable stick parity 0 = Disable stick parity
4	Parity select bit. Selects either an odd or even number of 1's to be transmitted/checked in the data word bit and parity bit. 0 = Odd number of 1's (parity bit is a logic 1, mark parity) 1 = Even number of 1's (parity bit is a logic 0, space parity)
3	Parity enable bit. The parity bit is used to produce an even or odd number of 1's when the data bits and the parity bit are summed. A parity bit is generated (transmit data) or checked (received data) between the last data bit and the stop bit of the serial data. 0 = Parity bit is not generated/checked 1 = Parity bit is generated/checked
2	Specifies the number of stop bits transmitted with each serial character. The receiver checks the first stop bit only, regardless of the number of stop bits selected. 0 = 1 stop bit 1 = 1.5 stop bits, when a 5-bit data length is selected 1 = 2 stop bits, when 6-, 7-, or 8-bit data length is selected
0-1	Specify the number of data bits (data length) in each transmitted or received serial character. The following are the bit values: 00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits

### Programmable Baud Generator

The UART contains two independently programmable baud generators. The 48-MHz crystal oscillator frequency input is divided by 26, resulting in a frequency of 1.8462-MHz. This is sent to each baud generator and divided by the divisor for the associated UART. The output frequency of the baud generator is  $16 \times$  the baud rate, [divisor # = (frequency input) / (baud rate  $\times$  16)]. The output of each baud generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These divisor latches must be loaded

during initialization to ensure proper operation of the baud generator. Upon loading either of the divisor latches, a 16-bit baud counter is loaded.

The table on the next page provides decimal divisors to use with crystal frequencies of 48-MHz. The oscillator input to the chip should always be 48-MHz to ensure that the FDC timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is not recommended.

### Line Status Register (LSR)

This register provides status information to the CPU concerning the data transfer. LSR is intended for read

operations only. Writing to this register is not recommended as this operation is only used for factory testing.

### Line Status Register Function Definition

Bit	Description
7	In FIFO, LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU read the LSR, if there are no subsequent errors in the FIFO.
6	This bit is the transmitter empty (TEMT) indicator. It is set to 1 whenever the transmitter holding register (THR) and the transmitter shift register (TSR) are both empty. It is reset to 0 whenever either the THR or TSR contains a data character.
5	<b>Transmitter Holding Register Empty (THRE) indicator.</b> Indicates that the UART is ready to accept a new character for transmission. It also causes the UART to issue an interrupt to the CPU when the THRE interrupt enable is set. This bit is set to 1 when a character is transferred from the THRE into the TSR. It is reset to 0 whenever the CPU loads the THRE.
4	<b>Break Interrupt (BI) indicator.</b> This bit is set to 1 when the received data input is held in the spacing (logic 0) state for longer than a full word transmission time (that is, the total time of start bit + data bits + parity + stop bits). It is reset whenever the CPU reads the contents of the LSR. Restarting after a break is received requires the SIN pin to be logical 1 for at least 1/2-bit time.
3	<b>Framing Error (FE) indicator.</b> This bit indicates that the received character did not have a valid stop bit. It is set to 1 whenever the stop bit following the last data bit or parity bit is a logic 0 (spacing level). The FE indicator is reset whenever the CPU reads the contents of LSR. The UART tries to resynchronize after a framing error. To do this, it assumes that the FE was due at the next start bit, so it samples this start bit twice and then takes in the data.
2	<b>Parity Error (PE) indicator.</b> This bit indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. It is set to 1 upon detection of a parity error and reset to 0 whenever the CPU reads the contents of the LSR.
1	<b>Overrun Error (OE) indicator.</b> This bit indicates that data in the RBR was not read by the CPU before the next data was transferred into the RBR, thereby destroying the previous data. It is set to 1 upon detection of an overrun condition and reset to 0 whenever the CPU reads the contents of the LSR.
0	<b>Receive Data Ready (DR) indicator.</b> This bit is set to 1 whenever a complete incoming character has been received and transferred into the RBR. It is reset to 0 by reading the data in the RBR.

**Table 1-19 Baud rates using 1.8462 MHz Clock (48 MHz/26)**

Desired baud rate	Decimal Divisor for 16X Clock	Percent Error	High speed mode bit in Index F0h
50	2304	0.1%	X
75	1536	0.2%	X
110	1047	0.2%	X
134.5	857	0.4%	X
150	768	0.2%	X
300	384	0.2%	X
600	192	0.2%	X
1200	96	0.2%	X
1800	64	0.2%	X
2000	58	0.5%	X
2400	48	0.2%	X
3600	32	0.2%	X
4800	24	0.2%	X
7200	16	0.2%	X
9600	12	0.2%	X
19200	6	0.2%	X
38400	3	0.2%	X
57600	2	0.2%	X
115200	1	0.2%	X
230400	32770	0.2%	1
460800	32769	0.2%	1

**Interrupt Identification Register (IIR)**

This register keeps a record of the four interrupts prioritized by the UART to reduce software overhead during data transfers. The four levels of interrupt conditions in order of priority are: receiver-line-status, received-data-ready, transmitter-holding-register-empty, and modem-status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete.

**Interrupt Identification Register**

Bit	Description
7~6	These two bits are set when the FIFO control register bit 0 equals 1.
5~4	Always '0'.
3	In non-FIFO mode, this bit is a logic 0. In FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.
2~1	Identifies the highest interrupt pending.
0	Used in an interrupt environment to indicate whether an interrupt condition is pending. If yes, the IIR contents may be used as a pointer to the appropriate interrupt service routine. 0 = Interrupt pending 1 = No interrupt pending

Table 1-20 Interrupt Control Table

FIFO mode only	Interrupt ID. register	Interrupt Set and Reset Functions			
		Priority level	Interrupt type	Interrupt source	Interrupt Reset control
D3	D2-D1-D0	-	None	None	-
0	0- 0- 1	-	None	None	-
0	1- 1- 0	highest	Receiver line status	Overrun error, Parity error, Framing error, Break interrupt	Reading the line status register
0	1- 0- 0	second	Received data available	Received data available	Read receiver buffer or the FIFO drops below the trigger level
1	1- 0- 0	second	Character timeout Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time.	Reading the Receiver Buffer Register
0	0- 1- 0	third	Transmitter holding register empty	Transmitter Holding Register Empty	Reading the IIR Register or writing the transmitter holding register
0	0- 0- 0	fourth	MODEM status	Clear to send or data set ready or Ring indicator or Data Carrier Detect	Reading the Modem status register

**Interrupt Enable Register (IER)**

This register enables the four types of UART interrupts. Each interrupt can individually activate the UART's IRQ output signals. Resetting bits 0 ~ 3 of the IER disables the interrupt system. Similarly, setting bits of this register to 1 enables the selected interrupts. Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the line status and modem status registers.

**Interrupt Enable Register Table**

Bit	Description
7-4	Always 0
3	Enables the modem-status interrupt
2	Enables the receiver-line-status interrupt
1	Enables the THRE interrupt
0	Enables the received-data-available interrupt

**FIFO Control Register**

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level.

**Bit 0:** Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. This bit must be a 1 when other FCR bits are written or they will not be programmed.

**Bit 1:** Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

**Bit 2:** Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

**Bit 3,4, 5:** FCR3 to FCR5 are reserved for future use.

**Bit 6, 7:** FCR6 and FCR7 are used to set the trigger level for the RCVR FIFO interrupt.

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14



**Modem Control Register (MCR)**

This register controls the interface with the modem or data set (or a peripheral emulating a modem).

**Modem Control Register**

Bit	Description
7~5	Set to logic 0.
4	<p>This bit provides a local loopback feature for the UART diagnostic testing. When set to 1, the following occurs: the transmitter serial output (SOUT) is set to the marking (1) state; the receiver serial input (SIN) is disconnected; the output of the transmitter shift register is looped back into the receiver shift register input; the four modem control inputs (DSRJ, CTSJ, RIJ, and DCDJ) are disconnected; and four Modem control outputs (DTRJ, RTSJ, OUT1J, IRQ) are internally connected to the four Modem control inputs. The modem control output pins are forced to their high (inactive) states. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-receive data paths of the serial port.</p> <p>In the diagnostic mode, the receiver and transmitter interrupts status are fully operational. Their sources are external to the part. The Modem Control interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem control inputs. The interrupts are still controlled by the Interrupt Enable Register.</p>
3	This bit enables the interrupt when set. In local loopback mode, this bit controls bit 7 of the MSR.
2	This is the OUT1 bit. It does not have a pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the MSR.
1	Controls the RTSJ output. In local loopback mode, this bit controls bit 4 of the MSR.
0	<p>Controls the DTRJ output. In local loopback mode, this bit controls bit 5 of the MSR.</p> <p>0 = DTRJ output is forced to 1</p> <p>1 = DTRJ output is forced to 0</p>

**Modem Status Register (MSR)**

This register gives the current state of the control lines between a modem and the CPU. The four LSB bits are set to

1 whenever a control input from the modem changes state, and set to 0 when the CPU reads the MSR.

**Modem Status Register**

Bit	Description
7	Complement of the DCDJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to IRQ enable in the MCR.
6	Complement of the RIJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.
5	Complement of the DSRJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to DTR in the MCR.
4	Complement of the CTSJ input. If bit 4 (loopback) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.
3	Delta data carrier detect (DDCD) indicator indicates that the DCDJ input to the chip has changed state. Whenever bit 0, 1, 2 or 3 is set to 1, a modem status interrupt is generated.
2	Trailing edge of ring indicator (TERI) detector indicates that the RIJ input of the chip has changed from a low to high state.
1	Delta data set ready (DDSR) indicator indicates that the DSRJ input to the chip has changed its state since the last time it was read by the CPU.
0	Delta clear to send (DCTS) indicator indicates that CTSJ input to the chip has changed its state since the last time it was read by CPU.

**Scratchpad Register (SCR)**

The 8-bit read/write register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

configuration space. Only UART2 can be programmed in this mode. The transfer signals will route to IRRX and IRTX.

**Infrared Interface**

The SOUTH BRIDGE provides pins with infrared communications capabilities. It operates in the following modes:

- Sharp-IR
- IrDA SIR
- IrDA MIR
- IrDA FIR

**Sharp-IR Mode**

This mode supports bi-directional data communication with a remote device using infrared radiation as the transmission medium. Sharp-IR uses Amplitude Shift Key (ASK) and allows serial communication at baud rates up to 38.4K Baud. The format of the serial data is similar to the UART data format, a zero value start bit, followed by up to 8 data bits, an optional parity bit, and ending with at least one stop bit with a binary value of one. A zero is signaled by sending a 500KHz continuous pulse train of infrared radiation. A one is signaled by the absence of any infrared signal.

The device operation in Sharp-IR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half-duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART's

**IrDA SIR Mode**

This is an operation mode similar to Sharp-IR. The IrDA 1.0 SIR allows serial communication at baud rates up to 115.2K Baud. The data format is the same as Sharp-IR mode except no parity bit is needed. A zero is signaled by sending a single infrared pulse. A one is signaled by not sending any pulse. The width of each pulse is 3/16ths of a single bit time. The device operation in IrDA 1.0 SIR mode is similar to the operation in UART. The main difference is that the data transfer is normally performed in half duplex fashion, and the modem control and status signals are not used. Selection of this mode is controlled by the IR mode bits in the UART's configuration space. All of the three UARTs can be programmed in this mode. The transfer signals will route to SIN1/SIN2/IRRX and SOUT1/SOUT2/IRTX.

**IrDA MIR and FIR**

The SOUTH BRIDGE supports both IrDA 1.1 MIR and FIR modes, with data rates of 0.576Mbps, 1.152Mbps and 4.0Mbps respectively. Details on the frame format, encoding schemes, CRC sequences, etc. are provided in the appropriate IrDA documents. The MIR and FIR communications are available on UART2 only and signals are routed to IRTX, IRRX, and IRRXH only.

**FIR Register Set**

Before accessing the FIR registers, the UART2 and FIR enable bits (bit 0 and bit 7) of index 0x30 in the UART2's configuration space must set to 1 first. After this, the user can switch between the conventional UART registers and FIR registers space by the procedure described below.

To change from the conventional space to FIR space, bits 7-5 of the MCR (Modem Control Register) are written to 001, 011, and 100 consecutively. And all of the four banks of FIR registers are available by switching between the bank select bits in the Master Control register. Writing one to bit 7 of the Master Control register will switch back to conventional UART register space immediately.

**Table 1-21 FIR Register Bank Summary**

Bank	Alias	Type	Register Name	Def n.
X	Base+7	R/W	FIR Master Control	00
0	Base+0	R/W	FIR DATA Register	00
0	Base+1	R/W	FIR Interrupt Enable	00
0	Base+2	RO	FIR Interrupt Identification	00
0	Base+3	R/W	FIR Line Control A	00
0	Base+4	R/W	FIR Line Control B	07
0	Base+5	R/W	FIR Line Status	00
0*	Base+6	R/W	FIR Bus Status	00
1	Base+0	R/W	FIR Configuration	00
1	Base+1	R/W	FIR FIFO Threshold	01
1*	Base+2	R/W	ISA DMA Threshold	00
1*	Base+3	R/O	FIFO Flag Register	00
1*	Base+3	W/O	Timer Interrupt Interval Register	11
1*	Base+4	R/O	FIFO Read Address	00
1*	Base+5	R/O	FIFO Write Address	00
1*	Base+6	WO	Test	00
2	Base+0	R/W	IrDA Control	00
2	Base+1	R/W	BOF Count	00
2	Base+2	R/W	Brick Wall Count	00
2	Base+3	R/W	TX DATA Size (high)	00
2	Base+4	R/W	TX DATA Size (low)	00
2	Base+5	R/O	RX DATA Size (high)	00
2	Base+6	R/O	RX DATA Size (low)	00
3	Base+0	R/O	FIR ID version	00
3	Base+1	R/W	FIR module control	N/A
3	Base+2	R/O	FIR higher I/O base address	N/A
3	Base+3	R/O	FIR lower I/O base address	N/A
3	Base+4	R/O	FIR IRQ channel	N/A
3	Base+5	R/O	FIR DMA channel	N/A

**Master Control Register**

This register is a read/write register and its default value is 00h. It is accessible regardless of which bank is on now. The definition of this register is described below.

Bit	Description
7	Register Space Switch. Writing a 1 to this bit will switch the FIR register space back to conventional UART space.
6	Master Reset. Setting the Master Reset bit resets all registers in FIR. The Master Reset bit will return to zero following the reset operation.
5	Master Interrupt Enable. Setting the Master Interrupt Enable bit to zero will disable all FIR interrupts regardless of the state of their individual enables.
4	Error Reset. Writing a one to the Error Reset bit will reset the FIR Line Status Register and reset the Message Count bits to zero. The Error Reset bit will return to zero following the reset operation.
3-2	Reserved
1-0	FIR Register Bank Select 0 0 : Bank 0 0 1 : Bank 1 1 0 : Bank 2 1 1 : Bank 3

**Bank 0 Registers****Alias 0, FIR Data Register (R/W)**

The Data register is the FIR FIFO access port. The FIR FIFO is written when transmitting and read when receiving. A host read is blocked when the FIFO is empty and a host write is blocked when the FIFO is full.

**Alias 1, FIR Interrupt Enable Register (R/W)**

Bit	Description
7	Active Frame Interrupt Enable
6	End of Message Interrupt Enable
5	Timer Interrupt Enable
4	FIR FIFO Interrupt Enable
3-0	Reserved

**Alias 2, FIR Interrupt Identification Register (Read only)**

Bit	Description
7	Active Frame Interrupt. When this bit is one, an Active Frame has occurred. The interrupt request (IRQ) line will go active when the Active Frame Interrupt Enable bit is set to one, the Master Interrupt Enable bit is set, and this bit is one.
6	End of Message Interrupt. When this bit is one, an End of Message has occurred. The EOM indicates that an IrDA FIR frame has transferred completely or been aborted. Reading the FIR Interrupt Identification Register will reset this bit. The interrupt request (IRQ) line will go active when the EOM Interrupt Enable bit is set to one, the Master Interrupt Enable bit is set, and this bit is one.
5	Timer Interrupt. When this bit is one, a timer interrupt has occurred. The timer interval can be programmed. There are four intervals that can be selected, they are 500 us, 1ms, 2ms, and 4ms.
4	FIR FIFO Interrupt. When this bit is one, a FIFO interrupt source has occurred. The FIR FIFO interrupt indicates that the FIR FIFO Interrupt enable is active and either a TxServReq or RxServReq has occurred. The FIR FIFO Interrupt bit is cleared when the interrupt source is inactive. That is, this bit would not be cleared by reading FIR Interrupt Identification Register. The interrupt request (IRQ) line will be active when the Master Interrupt Enable bit is set, and this bit is one.
3-0	Reserved.

**Alias 3, FIR Line Control Register A (R/W)**

Bit	Description
7	FIFO Reset. When setting this bit to one, the FIFO Full and Not Empty flags of the 32-byte FIR FIFO will be cleared. The FIFO Reset bit will return to zero automatically.
6-3	Reserved
2	Abort. When setting this bit to one, the current transmitting process will be terminated, the EOM flag is activated and the FIR FIFO is cleared. The Abort bit is reset by the End-of-Frame. The Abort is only used in transmit mode.
1	Data Done. The Data Done bit is used during transmitting to distinguish an end-of-valid-message-data condition (Data-Done-Bit=1) from a FIFO Underrun (Data-Done-Bit=0) that indicates incomplete message data. The Data Done bit is set by the host in PIO mode. The Terminal Count automatically activates the Data Done bit in the transmit DMA mode. The Data Done bit is automatically reset to zero at the end of a message only if the FIR FIFO is empty.
0	BWLF Set (Back to Back last frame set) When this bit is set, the last frame will end automatically, if the FIFO is empty. Thus this bit must be set at the last frame in Back to Back transfers.

**Alias 4, FIR Line Control Register B (R/W)**

Bit	Description															
7-6	<p>FIR Mode</p> <table><tr><th>Bit 7</th><th>Bit 6</th><th>Mode Description</th></tr><tr><td>0</td><td>0</td><td>Receive and Transmit both disable (default)</td></tr><tr><td>0</td><td>1</td><td>Transmit mode</td></tr><tr><td>1</td><td>0</td><td>Receive mode</td></tr><tr><td>1</td><td>1</td><td>Reserved</td></tr></table> <p>Transmission is active whenever TC goes active, or the FIFO Threshold has been exceeded.</p>	Bit 7	Bit 6	Mode Description	0	0	Receive and Transmit both disable (default)	0	1	Transmit mode	1	0	Receive mode	1	1	Reserved
Bit 7	Bit 6	Mode Description														
0	0	Receive and Transmit both disable (default)														
0	1	Transmit mode														
1	0	Receive mode														
1	1	Reserved														
5	SIP Enable. When the SIP Enable bit is set to one, a SIR Interaction Pulse will be asserted every 500ms if no transmitting or receiving has occurred.															
4	Brick Wall. The Data Size Register can also be used when the Brick Wall bit is active to send back-to-back IrDA FIR frames when the DMA data block is larger than the IrDA message length. In this case, if the maximum number of data bytes (according to the data size register) have been transferred and the DMA terminal count or FIFO Empty flags have not been activated, the next message is brick walled to the previous message.															
3-0	Message Count. The four Message Count bits controls hardware access to the Line Status Registers and are unaffected by the Status Register Address bits. The Message Count bits are incremented after an active frame.															

**Alias 5, FIR Line Status Register (R/W)**

There are eight FIR Line Status Registers. Bits 7-3 of each register are read-only and are accessed by programming the three FIR Line Status Address bits (bits 2-0). The status of all eight FIR Line Status registers are reset by a Master reset, Power-on-reset, and Error reset. The current FIR Line Status register pointed to by the Message Count will be reset following a valid IrDA BOF sequence.

Bit	Description
7	FIFO Under/Overrun (Read only). In transmit mode, the FIFO Underrun bit gets set to one when the transmitter runs out of the FIFO and the Data Done bit is not active. In receive mode, the FIFO Overrun gets set to one when the receiver tries to write data to the FIFO when the FIFO is full.
6	Frame Error (Read only). The Frame Error bit gets set to one when IrDA errors are detected.
5	Size Error (Read only). The Size Error gets set to one whenever the receiver decrements the RX Data Size count to zero before the End-of-Frame, or whenever the Brick Wall bit is inactive and the transmitter decrements the TX Data Size count to zero before FIFO Empty goes active.
4	CRC Error (Read only). The CRC Error bit gets set to one when the Frame-Check-Sequence errors have occurred in this receive message frame.
3	Frame Abort (Read only) The Frame Abort bit gets set to one when: 1) a forced abort, by setting the Abort bit of FIR Line Control Register A; 2) a FIFO underrun with the Data Done bit inactive during transmitting; 3) a FIFO overrun during receiving; 4) frame errors during receiving. Note: The Frame Abort bit will not go active during transmitting if the TX Data Size register decrements to zero when the last byte is read from the FIFO with the Data Done bit not set.
2-0	FIR Line Status Address (R/W) The Status Register Address bits control software read accesses to the eight FIR Line Status Registers at the same I/O address (alias 5, bank 0). To access any one of the eight FIR Line Status Registers, first write the address of the appropriate register (0-7), then read the appropriate register contents.

**Alias 6, FIR Bus Status Register (Read only)**

Bit	Description
7	FIFO Not Empty When this bit is one, there is one or more data words in the FIR FIFO.
6	FIFO Full When this bit is one, there is no room for loading data to the FIFO.
5	End of message
4	SIP assert bit. Reflection of the SIP signal.
3	Read Ready
2-0	Reserved

**Bank 1 Registers****Alias 0, FIR Configuration Register (R/W)**

Bit	Description
7-4, 2	Reserved
3	Timer enable. When this bit is set, the timer begins to count.
1	DMA Burst Mode. When the DMA Burst Mode bit is one, DMA Burst (Demand) mode is selected. When the DMA Burst Mode bit is zero, DMA Single Byte mode is selected.
0	DMA Enable. When the DMA Enable bit is one, the DMA host interface is active.

**Alias 1, FIR FIFO Threshold Register (R/W)**

Bit	Description
7-5	Reserved
4-0	FIR FIFO Threshold Bits The FIR FIFO Threshold bits contain the programmable FIFO threshold count. The threshold is from 0 to 31 for the FIR FIFO. If the data in FIFO is larger than the FIR FIFO threshold, the transfer starts in TX mode.

**Alias 2, FIR DMA Threshold Register (R/W)**

Bit	Description
7-5	Reserved
4-0	ISA DMA Threshold Bits ISA DMA transfer starts only if data in the FIFO is larger than the ISA DMA Threshold in the RX mode or if the data in the FIFO is smaller than the ISA DMA Threshold in the TX mode. The threshold is from 0 to 32 for the FIR FIFO.

**Alias 3, FIR Timer interrupt interval register(W/O)**

Bit	Description
7-2	Reserved
1-0	Timer interrupt scale register "00" => 500us, "01" => 1ms, "10" => 2ms, "11" => 4ms

**Alias 3, FIR FIFO Flag register (R/O)**

Bit	Description
7-6	Reserved
5-0	FIFO Flag Bits. These bits record the data in the FIFO.

**Alias 4, FIR FIFO Read Address register (R/O)**

Bit	Description
7-5	Reserved
4-0	FIFO Read address These bits are the current FIFO read address.

**Alias 5, FIR FIFO Write Address register (R/O)**

Bit	Description
7-5,	Reserved
4-0	FIFO Flag Bits. These bits are the current FIFO write address.

**Alias 6, Test register(WO)**

Bit	Description
7-0	Reserved for test only

**Bank 2 Registers****Alias 0, IrDA Control Register (R/W)**

Bit	Description												
7	1.152Mbps HDLC Select. This bit is used to select the bit rate in FIR HDLC mode. When the 1.152 Select bit is one, the IrDA 1.152Mbps HDLC-type FIR data rate is selected. Otherwise, the IrDA 0.576Mbps HDLC_type FIR data rate is selected.												
6	CRC Select. When the CRC Select bit is one, a hardware-generated CRC is appended to the transmitting frame between the data field and the STO flag. A hardware CRC checking sequence is also active during the receiving frame.												
5	HDLC select. When this bit asserts, HDLC mode is selected.												
4	HP mode (read only) If this bit is 1, the FIR is connected to an HP type transceiver module.												
3	SD/MODE State. When the SD/MODE State bit is one, the signal IRRXH is set to one. When the SD/MODE State bit is zero, the signal IRRXH is set to zero. The combination of this signal and IRTX will determine the operation speed of the transceiver module (IBM or TEMIC).												
2	FIR SIN Select. When the FIR SIN Select bit is zero, the input signal of the fast infrared data comes from the IRRX pin. When the SIN Select bit is one, the input signal of the fast infrared data comes from the IRRXH pin. When the SOUTH BRIDGE is used with an IBM (or TEMIC) transceiver module, IRRX is used as the infrared data input signal and SD/MODE will be used to control the speed of the module. When the SOUTH BRIDGE is used with an HP transceiver module, IRRX is used as the input signal of the serial infrared data and IRRXH is used as the input signal for the fast infrared data.												
1-0	SOUT State. These bits control the serial output signal (IRTX). <table><tr><th>Bit1</th><th>Bit0</th><th>SOUT signal state</th></tr><tr><td>0</td><td>X</td><td>Normal TX output signal</td></tr><tr><td>1</td><td>0</td><td>force to 0</td></tr><tr><td>1</td><td>1</td><td>force to 1</td></tr></table>	Bit1	Bit0	SOUT signal state	0	X	Normal TX output signal	1	0	force to 0	1	1	force to 1
Bit1	Bit0	SOUT signal state											
0	X	Normal TX output signal											
1	0	force to 0											
1	1	force to 1											

**Alias 1, BOF Count Register (R/W)**

The BOF Count register specifies the number of additional flags that are used in the BOF sequence of a frame, excluding brick wall frames. The BOF Count is an 8-bit value. The BOF means the STA flags in IrDA FIR HDLC (1.152/0.576Mbps) mode or the PAs in IrDA FIR 4PPM (4Mbps) mode.

**Alias 2, Brick Wall Count Register (R/W)**

The Brick Wall Count register specifies the number of additional interframe padding flags used for brick wall messages. The Brick Wall Count is an 8-bit value.

**Alias 3, TX Data Size Register (high) (R/W)**

Bit	Description
7-4	Reserved
3-0	TX Data Size High Byte

**Alias 4, TX Data Size Register (low) (R/W)**

Bit	Description
7-0	TX Data Size Low Byte. The TX Data Size count is 12-bit value. The TX Data Size registers specify the IrLAP-negotiated maximum number of payload data bytes per IrDA transmit message frame if the software CRC is selected, or the IrLAP-negotiated maximum number of payload data bytes minus the number of CRC bytes if hardware CRC is selected. The TX Data Size registers are used to 1) constrain the transmitter to a valid IrDA frame size, 2) simplify multi-frame windowing for transmit data blocks that are larger than the maximum packet size. If the TX Data Size registers are zero, the IrDA transmit message size is unlimited; i.e., the transmitter will operate until the FIR FIFO is empty.

**Alias 5, RX Data Size Register (high) (R/W)**

Bit	Description
7-4	Reserved
3-0	RX Data Size High Byte

**Alias 6, RX Data Size Register (low) (R/W)**

Bit	Description
7-0	RX Data Size Low Byte. The RX Data Size count is 12-bit value. The RX Data Size registers specify the IrLAP-negotiated maximum number of payload data bytes per IrDA receive message frame. The RX Data Size registers are used to check each IrDA FIR receive frame for a valid size. If the RX Data Size registers are zero, the IrDA receive message size is unlimited; i.e., a size error cannot occur because the receive frame size checking is disable.



**Bank 3 Registers****Alias 0, FIR ID Version Register (R/O)**

This register is used to distinguish the different versions of the FIR. The value is 00 in the SOUTH BRIDGE.

**Alias 1, FIR Module Control Register (R/W)**

Bit	Description
7	IR module type. This bit will control the type of connected IR module. This bit is a mirror of bit 7 in index 0xF0h of logical device 5.
6	This bit will reflect the signal on pin IRRXH. This is used for the detection of the IR module.
5-0	Read as 0.

**Alias 2, FIR Higher I/O Base Address Register (R/O)**

Bit	Description
7-0	Reflect the content of index 0x60h of the UART2.

**Alias 3, FIR Lower I/O Base Address Register (R/O)**

Bit	Description
7-3	Reflect the content of index 0x61h of the UART2.
2-0	Reserved.

**Alias 4, FIR IRQ Channel Register (R/O)**

Bit	Description
7-4	Reserved.
3-0	Reflect the content of index 0x70h of the UART2.

**Alias 5, FIR DMA Channel Register (R/O)**

Bit	Description
7-3	Reserved.
2-0	Reflect the content of index 0x74h of the UART2.

### 1.13 Keyboard Controller

The keyboard controller is a general-purpose 8-bit microcontroller. It is software compatible to the industry standard keyboard controller 8042AH. The controller consists of 256 bytes of data memory and 2K bytes of read-only program memory (ROM).

### Host System Interface

The keyboard controller is interfaced to the host system through a common system interface. The interface consists of SA15-0, AEN, SD7-0, IOWJ, IORJ, KIRQ and MIRQ for Keyboard and Mouse interrupts. The SOUTH BRIDGE decodes the keyboard controller chip-select at 60h and 64h. The following table shows the register address decoding utilized by the keyboard controller system interface.

Table 1-21 Summary of Sytem Interface Operations Table

ISA Address	IOWJ	IORJ	Operation
0x60	0	1	Data Write Buffer
	1	0	Data Read Buffer
0x64	0	1	Command Write Buffer
	1	0	Read Status Register

### Data Write Buffer

This is an 8-bit write only register. When written, the C/D status bit of the status register is cleared to zero and the IBF bit is set.

### Data Read Buffer

This is an 8-bit read only register. The Keyboard controller will set the OBF to 1 when the data is available. When read by the host, OBF bit will reset to 0.

### Command Write Buffer

This is an 8-bit write only register. When written, the C/D status bit of the status register is set to 1 and the IBF bit is set.

### Read Status Register

This is an 8-bit read only register and holds status information related to the system interface.

### Hardware Emulated Hotkey

The SOUTH BRIDGE also provides a hardware emulation hotkey algorithm for the convenience of waking up the system by pressing the keyboard or moving the mouse. There are three programmable keys for different combinations. Each key can be programmed as valid or not valid. One of the keys must be programmed as the last pressed key. When the system is powered down, the hardware will compare the make code received from the keyboard and generate a low pulse to turn on the power, like the power-on button on the front panel.

**1.14 Parallel Port****Parallel Port Interface**

The parallel interface is designed to provide all of the signals and registers needed to communicate using the IEEE1284 standard. It includes ISA-compatible and PS/2-compatible modes, EPP mode, and ECP mode. The programming of the base address, mode selection, and function disable for the Parallel Port can be found in Table 1-22.

Special circuitry is provided to protect against damage that might be caused when the printer is powered.

**Compatible Parallel Port**

The address decoding of the compatible parallel port registers utilizing A0 and A1 is shown below.

A1	A0	Port	Access
0	0	Data port	Read/Write
0	1	Status port	Read only
1	0	Control port	Read/Write
1	1	NIL	Tri-state

**Data Port**

This is a bi-directional data port that transfers 8-bit data. The direction is determined by bit 5 in the Control port. In the extended modes (PS/2-compatible, EPP, and ECP), bit 5 will determine the data direction in conjunction with the Read and Write strobes. In ISA-compatible mode, the parallel port operates in the output mode only.

**Status Port**

This register provides status for the signals listed below. It is a read only register. Writing to it is an invalid operation that has no effect on the Parallel Port.

**Bit 0 - Time-out Status**

When in EPP mode, this is the time-out status bit. When this bit is 0, no time-out occurs. When this bit is 1, a time-out has occurred on an EPP cycle (min. 10us). It is cleared to 0 after writing a "1" to this register. When not in EPP mode, this bit is 0.

Bits 1, 2 - are reserved bits. During a read of the Status register, these bits are 0.

**Bit 3 - Printer Error Status**

This bit represents the current state of the printer error signal (ERRORJ). The printer sets this low when there is a printer error. This bit follows the state of the ERRORJ pin.

**BIT 4 - Printer Selected Status**

This bit presents the current state of the printer select signal (SLCT). The printer sets this bit high when it is "On Line" and selected. This bit follows the state of the SLCT pin.

**Bit 5 - Paper End Status**

This bit represents the current state of the paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

**BIT 6 - Printer Acknowledge Status**

This bit represents the current state of the printer acknowledge signal (ACKJ). The printer pulses this signal low after it has received a character and is ready to receive another one. This bit follows the state of the ACKJ pin.

**BIT 7 - Busy Status**

This bit represents the current state of the printer busy signal. The printer sets this bit low when it is busy and cannot accept another character. This bit is the complement of the BUSY pin.

**Control Port**

This register provides all the output signals to control the printer except for bit 5.

**Bit 0 - Strobe Control**

This bit directly controls the data strobe signal to the printer via the STROBJ pin. This bit is the inverse of the STROBJ pin.

**Bit 1 - Autofeed Control**

This bit directly controls the automatic feed signal to the printer via the AUTOFDJ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the AUTOFDJ pin.

**Bit 2 - Initiate Control**

This bit directly controls the signal to initialize the printer via the INITJ pin. Setting this bit low initializes the printer. The INITJ pin follows this bit.

**Bit 3 - Printer Selected Input Control**

This bit directly controls the select in signal to the printer via the SLCTINJ pin. Setting this bit high selects the printer. It is the inverse of the SLCTINJ pin.

**Bit 4 - Interrupt Request Enable Control**

This bit controls the interrupt generated by the ACKJ signal. Its function changes slightly depending on the parallel port mode selected. In the following description, IRQx indicates the interrupt line allocated by the Parallel Port  
ISA-compatible and PS/2-compatible mode  
when bit 4=0, IRQx is floated  
when bit 4=1, IRQx follows ACKJ transitions.  
ECP and EPP mode  
when bit 4=0, IRQx is floated.  
When bit 4=1, IRQx is set active on ACKJ trailing edge

**Bit 5 - Direction Control**

Parallel control direction is valid in extended modes only. In ISA-compatible mode, the direction is always out regardless of the state of this bit. In extended modes, a logic 0 means that the printer port is in the output mode (forward direction); a logic 1 means that the printer port is in the input mode (reverse direction).

Bits 6 and 7 during a read are low, and cannot be written.

**Enhanced Parallel Port (EPP)**

EPP mode provides for greater throughput than compatible mode by supporting faster transfer time and a mechanism that allows the host to address peripheral device registers directly. Faster transfers are achieved by automatically generating the address and data strobes. EPP consists of eight single-byte registers as shown below. It also supports two operation modes: EPP1.7 and EPP1.9.

In Legacy mode, EPP is supported for a parallel port whose base address is 278h or 378h, but not for a parallel port whose base address is 3BCh. There are four EPP transfer operations: address write, address read, data write and data read. An EPP transfer operation is composed of a host read or write cycle and an EPP read or write cycle.

The software must write zero to bits 0,1 and 3 of the control register before executing EPP cycles, since the pins controlled by these bits are controlled by hardware during EPP accesses. Once these bits are reset to zero, the software may issue multiple EPP access cycles.

**EPP Operation**

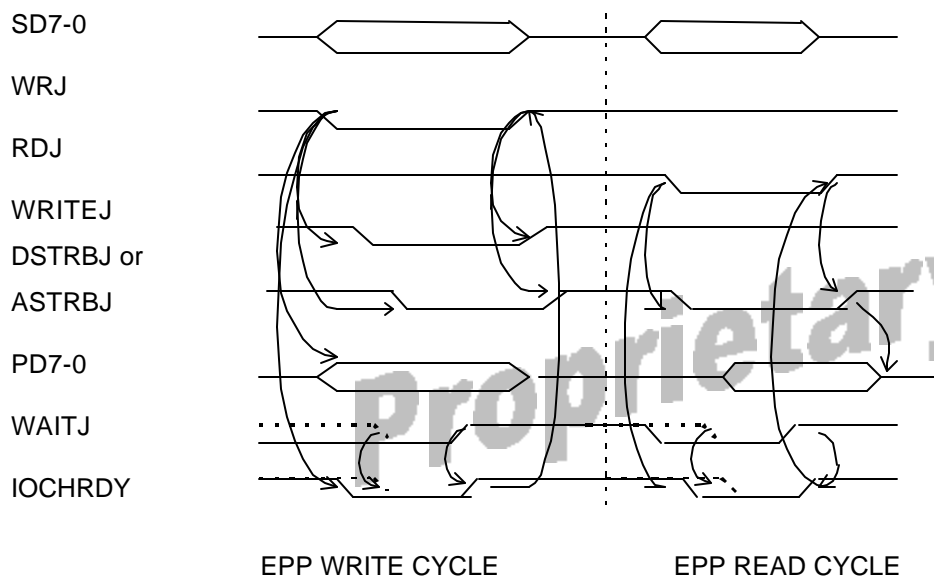
When the EPP mode is selected in the configuration register, the ISA-compatible and PS/2-compatible modes are also available. If no EPP read, write or address cycle is currently running, then the PD7-0 bus is in the compatible mode and all output signals (STROBJ, AUTOFDJ, INIT) are as set by the control register and direction is controlled by the direction bit in the control register.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system hang-ups. The timer indicates if more than 10 usec have elapsed from the start of the EPP cycle (IORJ or IOWJ asserted) and when the IOCHRDY will be deasserted. If a time-out condition occurs, the current EPP cycle is aborted and the time-out condition is indicated in the bit 0 of status register.

**Table 1-22**

Name	Offset	Mode	Type	Description
Compatible Data Register	0	SPP/EPP	R/W	This is the compatible mode data register.
Status Register	1	SPP/EPP	R	This is the status register.
Control Register	2	SPP/EPP	R/W	This is the control register.
EPP Address	3	EPP	R/W	This port is read/write. A write operation to it initiates an EPP device's register selection operation.
EPP Data Port 0	4	EPP	R/W	This is a read/write data port. It is used to transfer bits 7-0 in an 8-bit host bus interface.
EPP Data Port 1	5	EPP	R/W	This is the second EPP data port. It is used to transfer bits 8 to 15 in a 16-bit host bus interface.
EPP Data Port 2	6	EPP	R/W	This is the third EPP data port. It is used to transfer bits 16-23 in a 32-bit host bus interface.
EPP Data Port 3	7	EPP	R/W	This is the fourth EPP data port. It is used to transfer bits 23-31 in a 32-bit host bus interface.

EPP mode version 1.7 Timing



The timing for a Write/Read EPP 1.7 operation is shown in timing diagram above  
The sequence of operation is:

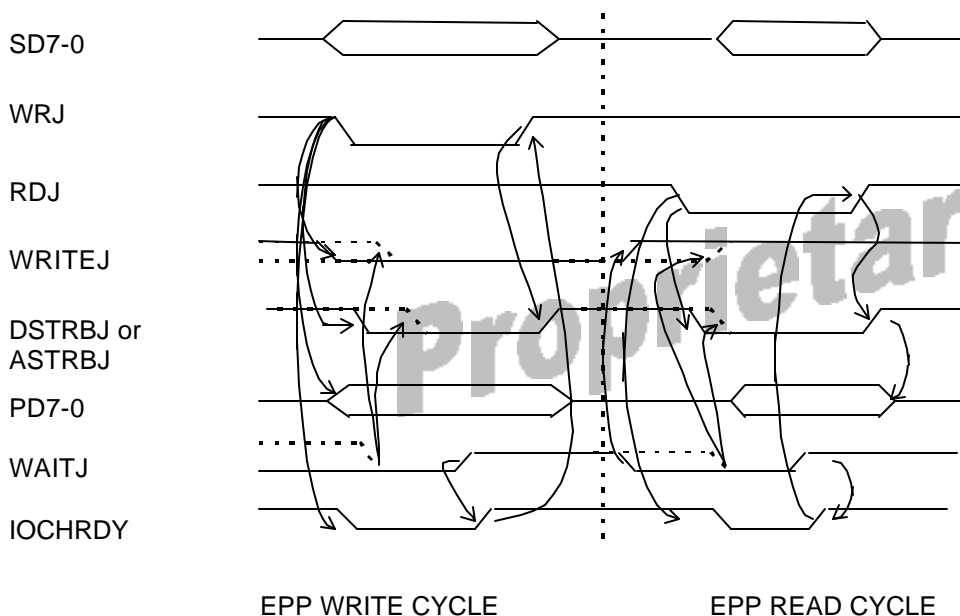
**EPP 1.7 Data/Address Write**

1. The host writes a byte to the Data (Address) port. WRJ goes low to drive data to PD7-0.
2. The EPP pulls WRITEJ low to indicate it's a write cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to signal that the data is valid.
4. If WAITJ goes low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then WRJ will go high
6. When WRJ goes high, it pulls WRITEJ & DSTRBJ (ASTRBJ) high, and then the EPP can change PD7-0

**EPP 1.7 Data/Address Read**

1. The host reads a byte from the Data (Address) port. RDJ goes low to input data from PD7-0.
2. The EPP keeps WRITEJ high to indicate it is a read cycle.
3. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that the peripheral has to start sending data.
4. If WAITJ is low during the cycle, IOCHRDY is pulled low.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high
6. When RDJ goes high, it pulls WRITEJ & DSTRBJ (ASTRBJ) high, and then the peripheral can tri-state PD7-0

## EPP mode version 1.9 Timing



The timing for a Write/Read EPP 1.9 operation is shown in timing diagram above  
The sequence of Write/Read operation is:

**EPP 1.9 Data/Address Write**

1. The host writes a byte to the Data (Address) port. WRJ goes low to drive data to PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low (or is already low), the EPP pulls (or keeps) WRITEJ low to indicate a write cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to indicate that data is ready and waits for WAITJ to go high.
5. When WAITJ goes high, it pulls IOCHRDY and DSTRBJ (ASTRBJ) high, and then WRJ will go high to turn off this cycle.

**EPP 1.9 Data/Address Read**

1. The host reads a byte from the Data (Address) port. RDJ goes low to input data from PD7-0.
2. IOCHRDY goes low and waits for WAITJ to go low.
3. If WAITJ goes low (or is already low), the EPP pulls (or keeps) WRITEJ high to indicate a read cycle.
4. The EPP pulls DSTRBJ (ASTRBJ) low to signal the peripheral to start sending data, and waits for WAITJ to go high.
5. When WAITJ goes high, the EPP pulls IOCHRDY high and then RDJ will go high.
6. When RDJ goes high, it pulls WRITEJ & DSTRBJ (ASTRBJ) high, and then the peripheral can tri-state PD7-0.

**Extended Capabilities Parallel Port****Introduction**

The ECP support includes a 16-byte FIFO that can be configured for either direction, command/data FIFO tags (one per byte), a FIFO threshold interrupt for both directions, FIFO empty and full status bits, automatic generation of commands and data cycle, and a RLE (run length encoding) expanding (decompression) as explained later.

The ECP is enabled through the configuration registers. Once enabled, its mode is controlled via bits 7-5 of the ECR register. The AFIFO, SDFIFO, and TFIFO registers access the same ECP FIFO. The FIFO can be accessed by host DMA cycles as well as host PIO cycles.

When DMA is configured and enabled (bit 3 of ECR is 1 and bit 2 of ECR is 0), the ECP automatically issues DMA requests to fill the FIFO (in the forward direction when bit 5 of DCR is 0) or to empty the FIFO (in the reverse direction when bit 5 of DCR is 1). All DMA transfers are to or from the FIFO. The ECP does not assert DMA request for more than 32 consecutive DMA cycles. The ECP stops requesting DMA when TC is detected during an ECP DMA cycle.

Please refer to the IEEE1284 Extended Capabilities Port Protocol document and ISA Interface Standard for software operation details.

**Register Description**

This section contains the registers used in the ECP mode. The I/O address alignment for this register set is shown below and the register descriptions are as follows:

**DATAR and AFIFO**

Modes 000 and 001 (Data Register)

The Data Register latches the contents of the data bus on the rising edge of the IOWJ input. The contents of this register are buffered and output to the PD7-0. During a read operation, PD7-0 is read and output to the host CPU.

Mode 011 (ECP Address/RLE FIFO)

This register provides a channel address or a Run Length Count to the peripheral, depending on the state of bit 7. The bytes written to this register are placed in the FIFO and transmitted over PD7-0 using ECP protocol. The peripheral device should interpret bit 6-0 as a channel address when bit 7=1 and as a run length count when bit 7=0. The SOUTH BRIDGE will assert AUTOFDJ low to indicate that the information on PD7-0 represents a command (address/RLE). The AUTOFDJ signal will drive high when PD7-0 is transferring data.

**Status Register (DSR)**

Please refer to Section 1.11.1.

**Control Register (DCR)**

Please refer to Section 1.11.1. Note that the bit 0 of DCR is written to 0 in mode 010 and 011 because the STROBJ signal is controlled by hardware. Bit1 of the DCR is written to 0 in mode 011 also. Additionally, in modes 010 and 011, bit 4 of DCR should be set to 0 to stop the generation of interrupts via the ACKJ signal.

**SDFIFO (Standard Parallel Port Data FIFO)**

Bytes written or direct memory accessed from the system to this FIFO are transmitted by a hardware handshake to the peripheral device using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

**Table 1-23**

Name	Address	I/O	Mode type (bit 7-5 of ECR)	Function
DATAR	Base+000h	R/W	000,001	Data register.
AFIFO	Base+000h	W	011	ECP address FIFO.
DSR	Base+001h	R	all	Status register.
DCR	Base+002h	R/W	all	Control register.
SDFIFO	Base+400h	W	010	Standard Parallel Port data FIFO.
DFIFO	Base+400h	R/W	011	ECP data FIFO.
TFIFO	Base+400h	R/W	110	TEST FIFO.
CNFGA	Base+400h	R	111	Configuration register A.
CNFGB	Base+401h	R	111	Configuration register B.
ECR	Base+402h	R/W	all	Extended control register.

**DFIFO (ECP Data FIFO)**

In the forward direction (bit 5 of DCR is 0), a byte written, or DMAed, to this register is pushed into the FIFO and tagged as data. The data is transmitted by a hardware handshake to the peripheral device using the ECP parallel port protocol.

In the backward direction (bit 5 of DCR is 1) the ECP automatically issues ECP read cycles to fill the FIFO. Reading this register pops a byte from the FIFO.

**TFIFO (Test FIFO Mode)**

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. However the ECP does not issue an ECP cycle to transfer the data to or from the device.

The TFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full TFIFO, the new data is not accepted into the TFIFO. If an attempt is made to read data from an empty TFIFO, the last data byte is re-read again. Data bytes are always read from the head of TFIFO regardless of the value of the direction bit. For example, if 44h, 33h, 22h is written to the FIFO, then reading the FIFO will return 44h, 33h, 22h in the same order as was written.

**CNFGA (Configuration Register A)**

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

**CNFGB (Configuration Register B)**

Bit 7 - compress

This bit is read only. During a read, it is a low level. This means that this chip does not support hardware RLE compression. It only supports hardware de-compression.

Bit 6 - IntrValue

Returns the value on the ISA IRQ line.

Bits 5~0 - These bits reflect the IRQ and DRQ selected by the configuration register.

IRQ selected	Config.Reg. B Bits 5: 3	DMA selected	Config.Reg. B Bits 2: 0
14	110	3	011
13	101	2	010
11	100	1	001
10	011	Others	000
9	010		
7	001		
5	111		
Others	000		

**ECR (Extended Control Register)**

This register controls the extended ECP parallel port functions.

Bits 7, 6, 5

These bits are Read/Write and select the operation mode

000: ISA-compatible mode. Write cycles are performed under software control. The FIFO is reset.

001: PS/2-compatible mode. Read and write cycles are performed under software control. The FIFO is reset.

010: ISA-compatible FIFO mode. Write cycles are performed under hardware control (STROBJ is controlled by hardware). Bit 5 of DCR is forced to 0 internally and PD7-0 are driven.

011: ECP mode. The FIFO direction is controlled by bit 5 of DCR. Read and write cycles to the device are performed under hardware control (STROBJ and AUTOFDJ are controlled by hardware).

100: EPP mode. In this mode, EPP is selected if the Parallel Port mode select bits in the configuration register are set to 011 (EPP1.9) or 111 (EPP1.7).

101: Reserved.

110: FIFO test mode. The FIFO is accessible via the TFIFO register. The ECP does not issue ECP cycles to fill or empty the FIFO.

111: Configuration mode. The CNFGA and CNFGB registers are accessible in this mode.

Bit 4 - ECP ERRORJ interrupt mask bit.

When this bit is 0, an interrupt is generated on the high-to-low edge of the ERRORJ signal. The ERRORJ signal is used by the peripheral device to request a reverse transfer. An interrupt is also generated when ERRORJ is asserted while this bit is changed from 1 to 0. This prevents the loss of an interrupt between ECR reads and ECR writes. When this bit is 1, no interrupt is generated.

Bit 3 - ECP DMA enable bit

0: Disable DMA unconditionally.

1: Enable DMA (DMA starts when bit 2 of ECR is 0).

BIT 2 - ECP service interrupt mask/status bit.

When this bit is written to 0 and one of the three interrupt events occur, an interrupt is generated and this bit is set to 1 by hardware.

- 1) Bit 3 of ECR is 1 and TC is reached during DMA.
- 2) Bit 3 of ECR is 0 and bit 5 of DCR is 0 (forward direction) and there are free bytes in the FIFO which are equal or greater than the threshold value. A threshold value of 0 means the interrupt is generated when the FIFO is empty.
- 3) Bit 3 of ECR is 0 and bit 5 of DCR is 1 (reverse direction) and there are valid bytes in the FIFO which are equal or greater than the threshold value. A threshold value of 0 means the interrupt is generated when the FIFO is full.

When this bit is written to 1, DMA and the above three interrupts are disabled. Writing 1 to this bit does not cause an interrupt.



Bit 1 - FIFO full bit (read only)

0: The FIFO has at least 1 free byte.

1: The FIFO is full.

Bit 0 FIFO empty bit (read only)

0: The FIFO contains at least 1 byte of data.

1: The FIFO is empty.

#### **ISA-compatible and PS/2-compatible Modes (mode 000 and 001)**

The software generates cycles by modifying the DCR register and reading the DSR register. The negotiation phase in the ECP mode are also performed in these modes.

#### **ISA-compatible FIFO mode (mode 010)**

The ISA-compatible mode uses the same signaling protocol on the parallel port interface as the ISA-compatible mode. However, there are two major operational differences. First data is written to a 16-byte FIFO via SDFIFO location. The FIFO empty and full bits in the ECR provide FIFO status. In addition, DMA can be used to transfer data to the FIFO by enabling this feature in the ECR. Second, the data is transferred to the peripheral using an automatic hardware handshake. This handshake emulates the standard ISA-compatible style software generated handshake. In this mode, the monitoring of the ACKJ signal is not required. Interrupts are enabled and reported via the ECR (bit 2). The generation of interrupts is based on the state of the FIFO and not individual transfers (using ACKJ) as in the standard ISA-compatible mode.

#### **ECP mode (mode 011)**

In ECP mode, both data and commands (address/RLE) are transferred using the FIFO. This information can be either written or read from the FIFO using DMA or non-DMA ISA bus transfers. The parallel port interface transfers use an automatic handshake protocol. The host controls the transfer direction by programming the direction bit in the DCR.

When the host is writing to the device (forward direction), STROBJ and BUSY provide the automatic handshake for transfers on the parallel port interface. AUTOFDJ indicates whether PD7-0 contain data (AUTOFDJ is high) or a command (AUTOFDJ is low). For commands, the host writes to the AFIFO and for data the host writes to the DFIFO.

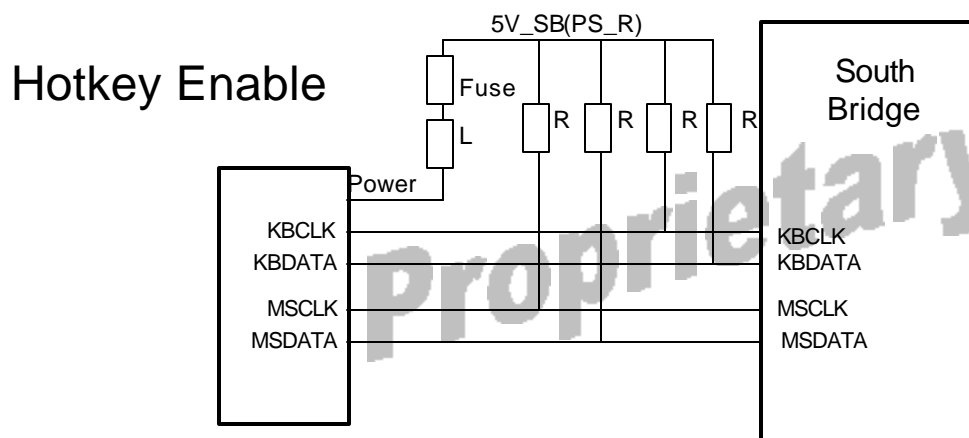
When the host is reading from the device (reverse direction), AUTOFDJ and ACKJ provide the automatic handshake for transfers on the parallel port interface. Data/commands from the device are placed in the DFIFO using this handshake. In this case, BUSY indicates whether PD7-0 contain data (BUSY is high) or a command (BUSY is low).

#### **Test Mode (mode 111)**

This mode is for testing the FIFO in PIO and DMA cycles. Both read and write operations are supported, regardless of the direction bit. It can be used to measure the host to ECP cycle throughput, usually with DMA cycles. This mode can also be used to check the FIFO depth and its interrupt threshold, usually with PIO cycles.

## 1.15 Hotkey Function Implementation

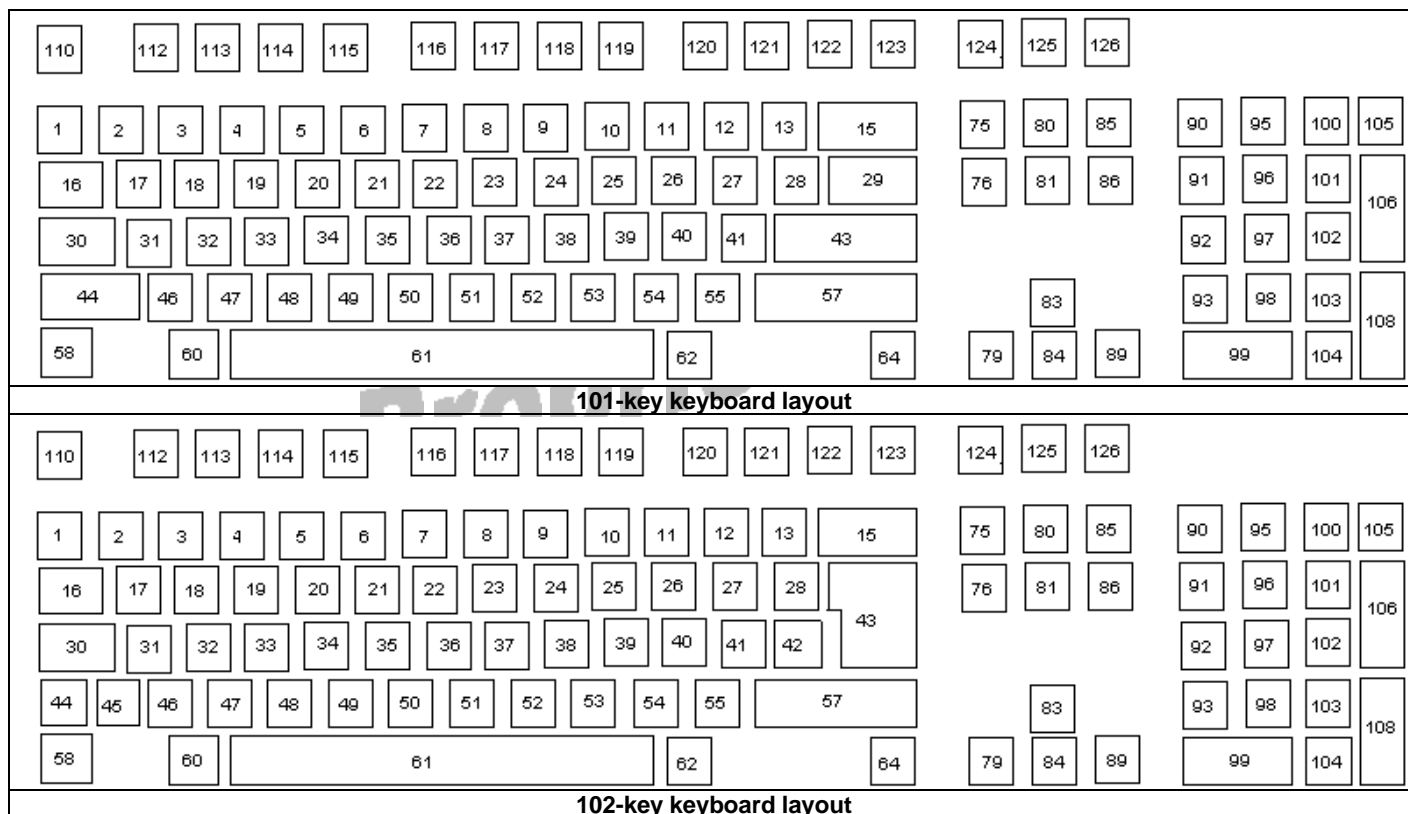
## 1.15.1 Hotkey Hardware Design Guide



## 1.15.2 Hotkey Programming Guide

1. The Super I/O supports Keyboard and Mouse Hotkey Event functions. The active Hotkey event will generate SMI/SCI or Resume Events to wake up from states S1-S5.
2. Set Super I/O logical device C index 30h bit0 to 1 to enable Keyboard Hotkey function.
3. Set Super I/O logical device C index 30h bit1 to 1 to enable Mouse Hotkey function.
4. Super I/O logical device C index F0h is suggested to use the default value
5. Write three make codes into the Super I/O logical device C index F1h, F2h, F3h to define which key combination is the hotkey.
6. The suggested value of Super I/O logical device C index F4h is 82h.

## 1.16 Keyboard Scan Codes and Make Codes



## Scan Codes

The following tables list the key numbers of the three scan code sets and their hexadecimal values.

### Scan Code Tables

In scan code, each key is assigned a unique 8-bit make scan code, which is sent when the key is pressed. Each key also sends a break code when the key is released. The break code consists of 2 bytes, the first of which is the break code prefix (hex F0). The second byte is the same as the make scan code for that key. The typematic scan code for a key is the same as the make code.

The following charts show the keys and the scan codes the keys send, regardless of any shift states in the key board or the system.

**Keyboard Scan Codes (Part 1 of 5)**

Key no.	Make Code	Break Code	Key no.	Make code	Break code
1	0E	F0 0E	47	22	F0 22
2	16	F0 16	48	21	F0 21
3	1E	F0 1E	49	2A	F0 2A
4	26	F0 26	50	32	F0 32
5	25	F0 25	51	31	F0 31
6	2E	F0 2E	52*	3A	F0 3A
7	36	F0 36	53	41	F0 41
8*	3D	F0 3D	54*	49	F0 49
9*	3E	F0 3E	55	4A	F0 4A
10*	46	F0 46	57	59	F0 59
11	45	F0 45	58	14	F0 14
12*	4E	F0 4E	60	11	F0 11
13*	55	F0 55	61	29	F0 29
15	66	F0 66	62	E0 11	E0 F0 11
16	0D	F0 0D	64	E0 14	E0 F0 14
17	15	F0 15	90	77	F0 77
18	1D	F0 1D	91	6C	F0 6C
19	24	F0 24	92	6B	F0 6B
20	2D	F0 2D	93	69	F0 69
21	2C	F0 2C	96	75	F0 75
22	35	F0 35	97	73	F0 73
23*	3C	F0 3C	98	72	F0 72
24*	43	F0 43	99	70	F0 70
25*	44	F0 44	100	7C	F0 7C
26	4D	F0 4D	101	7D	F0 7D
27	54	F0 54	102	74	F0 74
28	5B	F0 5B	103	7A	F0 7A
29**	5D	F0 5D	104	71	F0 71
30	58	F0 58	105	7B	F0 7B
31	1C	F0 1C	106	79	F0 79
32	1B	F0 1B	108	E0 5A	E0 F0 5A
33	23	F0 23	110	76	F0 76
34	2B	F0 2B	112	05	F0 05
35	34	F0 34	113	06	F0 06
36	33	F0 33	114	04	F0 04
37*	3B	F0 3B	115	0C	F0 0C
38*	42	F0 42	116	03	F0 03
39*	4B	F0 4B	117	0B	F0 0B
40*	4C	F0 4C	118	83	F0 83
41	52	F0 52	119	0A	F0 0A
42***	5D	F0 5D	120	01	F0 01
43*	5A	F0 5A	121	09	F0 09
44	12	F0 12	122	78	F0 78
45***	61	F0 61	123	07	F0 07
46	1A	F0 1A	125	7E	F0 7E

\* See 84/85-key keyboard in this section

\*\* Key 29 on US keyboards only

\*\*\* Keys 42 and 45 on all but US keyboards.

## Keyboard Scan Codes, 84/85 Numeric keypad

Key no.	Make Code	Break Code	Key no.	Make code	Break code
8	47	C7	25	4D	CD
9	48	C8	37	4F	CF
10	48	C9	38	50	D0
12	4A	CA	39	51	D1
13	4E	CE	40	37	B7
23	4B	CB	52	52	D2
24	4C	CC	54	53	D3

The remaining keys send a series of codes dependent on the state of the shift keys (Ctrl, Alt and Shift) and the state of Num Lock (On or Off). Because the base scan code is identical to that of another key, an extra code (hex E0) has been added to the base code to make it unique.

The following charts show the make/break code using the left Shift key. If the right Shift key is used, substitute its make/break code for that of the left Shift key.

**Keyboard Scan Codes (part 2 of 5)**

Key no.	Base Case, or Shift +Num Lock make/break	Shift case Make/break	Num Lock on Make/Break
75	E0 70 /E0 F0 70	E0 F0 12 E0 70 /E0 F0 70 E0 12	E0 12 E0 70 /E0 F0 70 E0 F0 12
76	E0 71 /E0 F0 71	E0 F0 12 E0 71 /E0 F0 71 E0 12	E0 12 E0 71 /E0 F0 71 E0 F0 12
79	E0 6B /E0 F0 6B	E0 F0 12 E0 6B /E0 F0 6B E0 12	E0 12 E0 6B /E0 F0 6B E0 F0 12
80	E0 6C /E0 F0 6C	E0 F0 12 E0 6C /E0 F0 6C E0 12	E0 12 E0 6C /E0 F0 6C E0 F0 12
81	E0 69 /E0 F0 69	E0 F0 12 E0 69 /E0 F0 69 E0 12	E0 12 E0 69 /E0 F0 69 E0 F0 12
83	E0 75 /E0 F0 75	E0 F0 12 E0 75 /E0 F0 75 E0 12	E0 12 E0 75 /E0 F0 75 E0 F0 12
84	E0 72 /E0 F0 72	E0 F0 72 E0 72 E0 F0 12 E0 7D	E0 12 E0 72 /E0 F0 72 E0 F0 12
85	E0 7D /E0 F0 7D	E0 F0 12 E0 7D /E0 F0 7D E0 12	E0 12 E0 7D /E0 F0 7D E0 F0 12
86	E0 7A /E0 F0 7A	E0 F0 12 E0 7A /E0 F0 7A E0 12	E0 12 E0 7A /E0 F0 7A E0 F0 12
89	E0 74 /E0 F0 74	E0 F0 12 E0 74 /E0 F0 74 E0 12	E0 12 E0 74 /E0 F0 74 E0 F0 12

**Keyboard Scan Codes (part 3 of 5)**

Key no.	Scan Code Make/Break	Shift Case Make/Break
95	E0 4A /E0 F0 4A	E0 F0 12 4A/E0 12 F0 4A

**Keyboard Scan Codes (part 4 of 5)**

Key no.	Scan Code Make/Break	Ctrl Case, Shift Case Make/Break	Alt Case Make/Break
124	E0 12 E0 7C /E0 F0 7C E0 F0 12	E0 7C /E0 F0 7C	84/F0 84

**Keyboard Scan Codes (part 5 of 5)**

Key no.	Make Code	Ctrl key Pressed
126*	E1 14 77 E1 F0 14 F0 77	E0 7E E0 F0 7E

\*This key is not typematic. All associated scan codes occur on the make of the key.

## Section 2 : Electrical Characteristics

## 2.1 FDC AC Characteristics

TA = 0°C to +70°C, VDD = +5V ± 10%.

All AC timings can be met with current loads that do not exceed 3.2 mA or -8 uA at 100 pF capacitive loading. For capacitive loads that exceed 100 pF, the following typical derating factors should be used:

100 pF < CL ≤ 150 pF, t = (0.10 ns/pF) (CL - 100 pF) typical  
 150 pF < CL ≤ 200 pF, t = (0.08 ns/pF) (CL - 100 pF) and  
 t = (0.5 ns/mA) (ISINK mA) or t = -(0.5 ns/mA) (ISOURCE mA)  
 tSOURCE is always negative, ISINK ≤ 4.8 mA, ISOURCE ≤ -120 uA, CL ≤ 250 pF.

Table 2-1 lists the AC Characteristics of the SOUTH BRIDGE.

**Table 2-1 AC Characteristics**

Symbol	Parameter	Conditions	Min	Max	Unit
tAR	Delay from address to RDJ		19		ns
tAW	Delay from address to WRJ		19		ns
tCH	Duration of clock high pulse	see Note A	16		ns
tCL	Duration of clock low pulse	see Note A	16		ns
tDH	Data hold time		10		ns
tDS	Data setup time		19		ns
tHZ	RDJ to floating data delay	see Note B	13		ns
tRA	Address hold time from RDJ		0		ns
tRC	Read cycle update		36		ns
tRD	RDJ strobe width		60		ns
tTPS	Port setup		13		ns
tRI	Read strobe to clear IRQ6		52		ns
tRVD	Delay from RDJ to data		31		ns
tRW	Reset pulse width		100		ns
tWA	Address hold time from WRJ		0		ns
tWC	Write cycle update		36		ns
tWI	Write strobe to clear IRQ6		52		ns
tWO	Write to output		41		ns
tWR	WRJ strobe width		50		ns
RC	Read cycle = tAR + tRD + tRC		115		ns
WC	Write cycle = tAW + tWR + tWC		105		ns

**Note:** A. Clock is derived from USB clock/2 (24 MHz maximum).

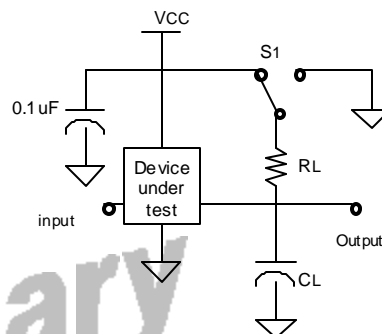
B. Charge and discharge time is determined by  $V_{OL}$ ,  $V_{OH}$  and the external loading.

## 2.2 AC Test Conditions

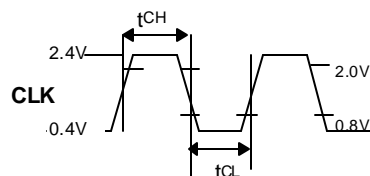
In Table 2-4,  $CL = 100\text{ pF}$ . This includes jig and scope capacitance. S1 is open for push-pull outputs. S1 is equal to VCC for high impedance to active low, and active low to high impedance measurements. S1 is equal to GND for high impedance to active high, and active high to high impedance measurements.  $RL = 1.0\text{ kohm}$  for CPU interface pins. For the open drain drive interface pins  $S1 = VCC$  and  $RL = 150\text{ ohms}$ .

Table 2-2 AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	6 ns
I/O reference levels	1.3V
Tri-state reference levels	Active high - 0.5V Active low + 0.5V



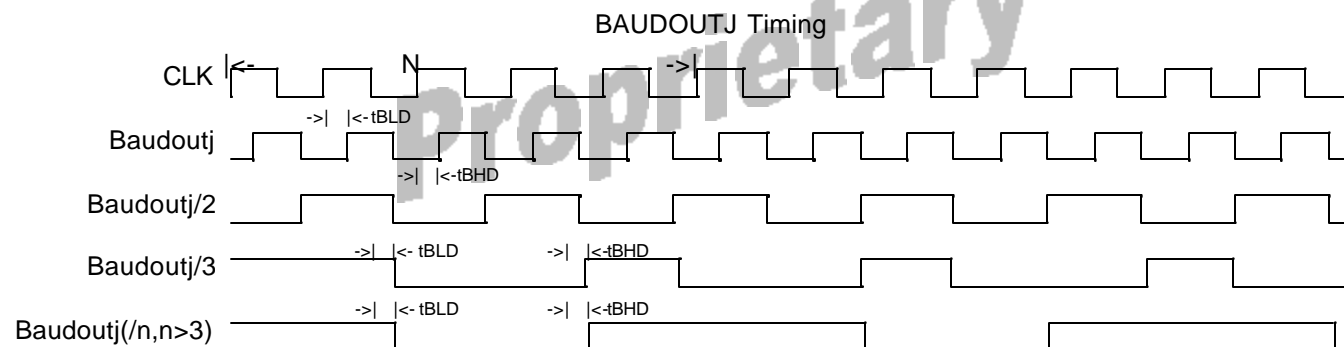
Clock Input = USB clock/2(24 MHz)



The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing

Table 2-3 Serial Interface Baud Generator

Symbol	Parameter	Conditions	Min <sup>16</sup>	Max	Unit
N	Baud Divisor		12 - 1		
tBHD	Baud output positive edge delay	CLK = 48 MHz / 4, 100 pF load		56	ns
tBLD	Baud output negative edge delay	CLK = 48 MHz / 4, 100 pF load		56	ns

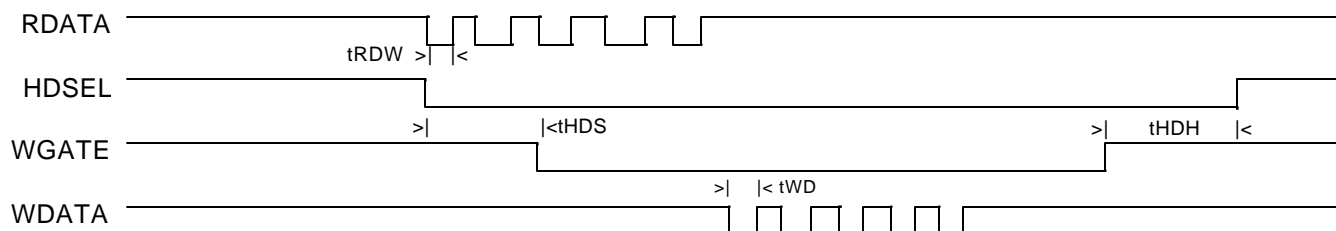


## Drive Read and Write Timing

Table 2-4 Drive Read and Write Timing

Symbol	Parameter	Conditions	Min	Unit
tRDW	Read-data pulse-width		25	ns
tWD	Write-data pulse-width	250 kb/s (MFM)	500	ns
tHDS	Head-select setup to write-gate-assertion		40	us
tHDH	Head-select hold from write-gate		12	ns
		300 kb/s (MFM)	416	ns
		500 kb/s (MFM)	250	ns
		1000 kb/s (MFM)	225	ns

**Note :** Whenever WGATE is asserted, the WDATA line is active. At the end of each write, one dummy byte is written before WGATE is deasserted.

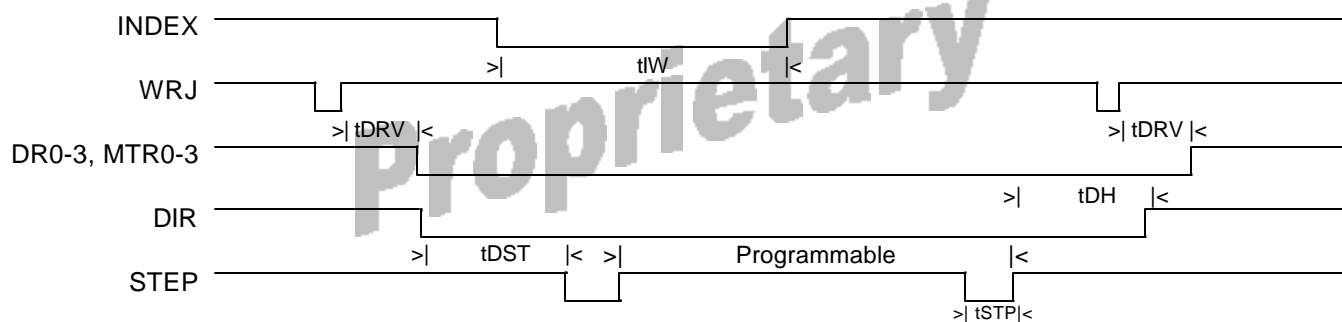




## Drive Track Access Timing

Table 2-5 Drive Track Access Timing

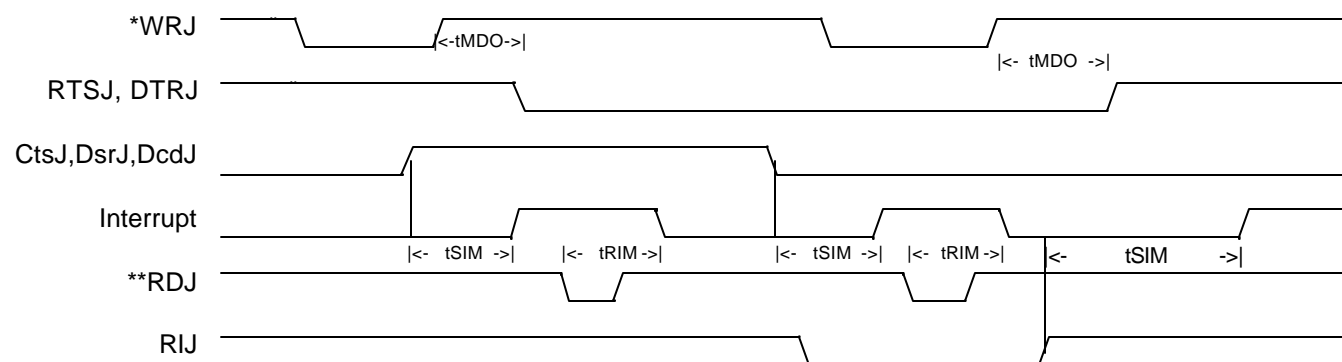
Symbol	Parameter	Min	Max	Unit
tDH	Direction hold from end-of-step	1		step time
tDRV	Drive-select or motor-time from write-strobe		100	ns
tDST	Direction-setup prior to step	6		us
tIW	Index pulse-width	100		ns
tSTP	Step pulse-width	8		us



## Modem Control

Table 2-6 Modem Control

Symbol	Parameter	Max	Unit
tMDO	Delay from WRJ (WR MCR) to output	50	ns
tRIM	Delay to reset interrupt from RDJ (RD MSR)	98	ns
tSIM	Delay to set interrupt from modem input	50	ns



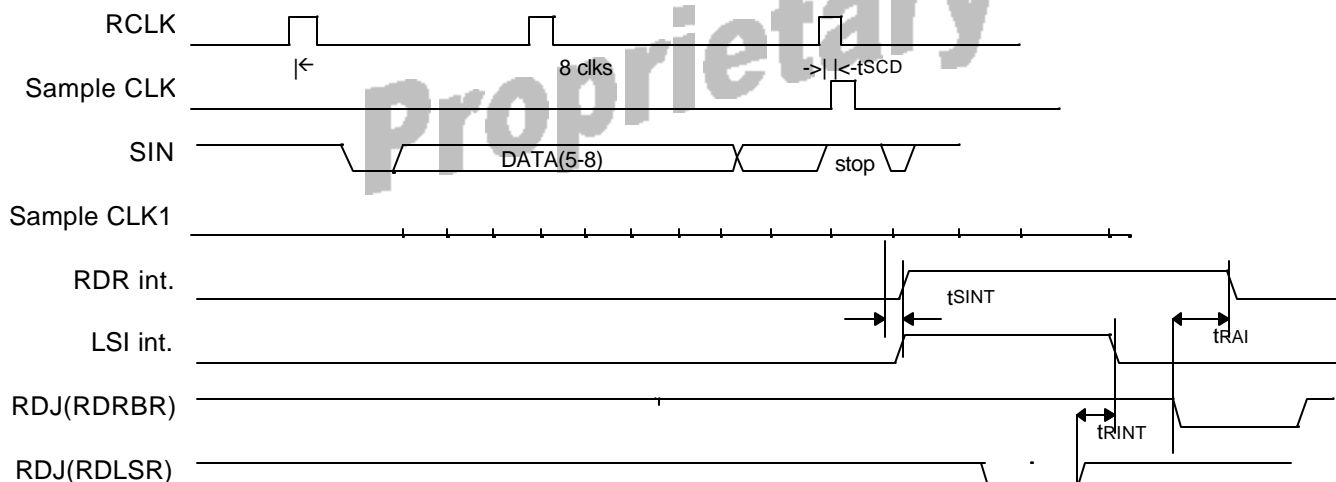
\* : See Write Cycle Timing

\*\* : See Read Cycle Timing

## Receiver

Table 2-7 Receiver

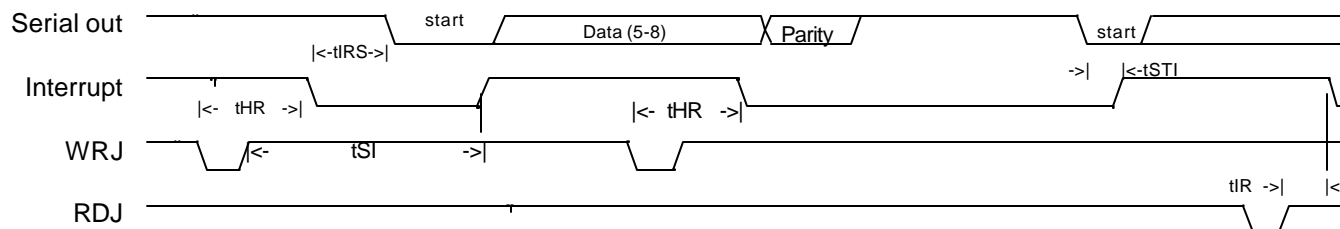
Symbol	Parameter	Max	Unit
$t_{RAI}$	Delay from active edge of RDJ to reset interrupt	98	ns
$t_{RINT}$	Delay from inactive edge of RDJ (RD LSR) to reset interrupt	50	ns
$t_{SCD}$	Delay from RCLK to sample time	41	ns
$t_{SINT}$	Delay from stop to set interrupt	2	Baudout cycles



## Transmitter

Table 2-8 Transmitter

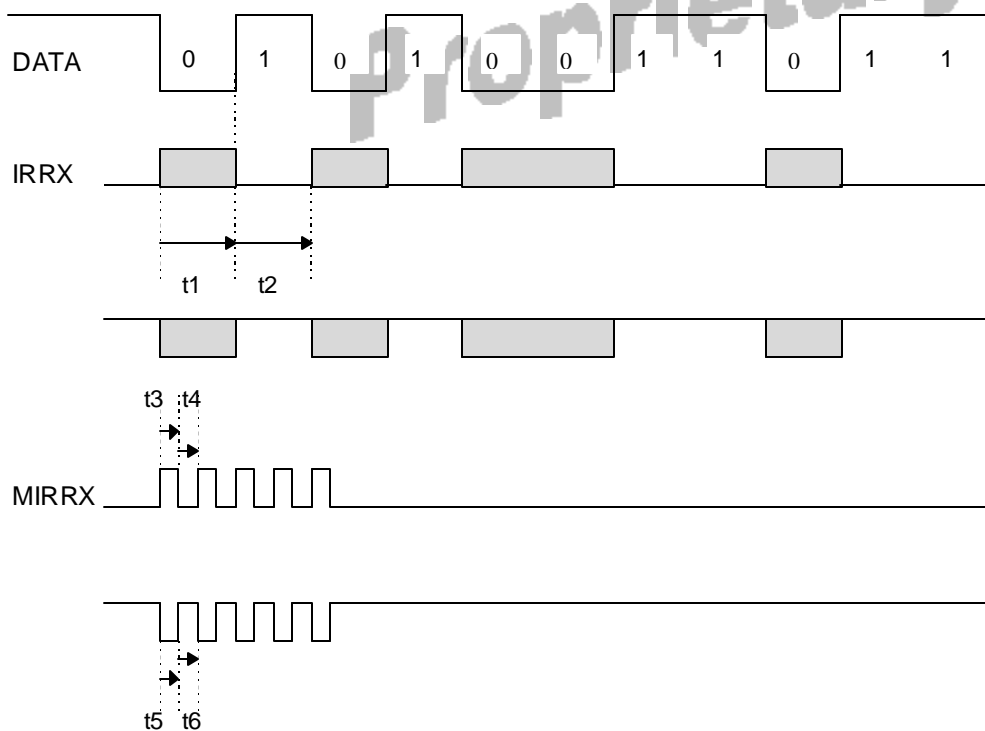
Symbol	Parameter	Min	Max	Unit
tHR	Delay from WRJ (WR THR) to reset interrupt		50	ns
tIR	Delay from RDJ (RD IIR) to reset interrupt (THRE)		50	ns
tIRS	Delay from initial INTR reset to transmit start	8	24	Baudout cycles
tSI	Delay from initial write to interrupt	16	24	Baudout cycles
tSTI	Delay from start to interrupt (THRE)		8	Baudout cycles



Amplitude Shift Keyed IR Receive Timing

Table 2-9. ASK IR Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Modulated output bit time				us
t2	Off bit time				us
t3	Modulated output "off"	0.8	1	1.2	us
t4	Modulated output "on"	0.8	1	1.2	us
t5	Modulated output "on"	0.8	1	1.2	us
t6	Modulated output "off"	0.8	1	1.2	us



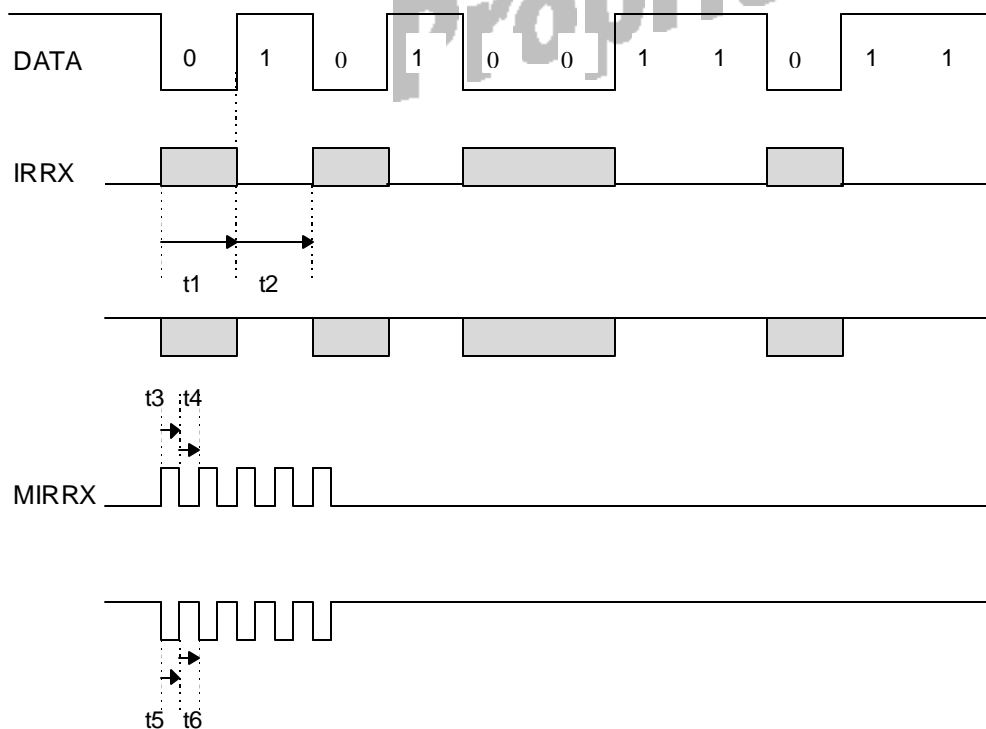
Notes :

1. t1, t2 timing referred to IrDA Receive Timing @ each baud rate.
2. UART1, UART2, UART3 0xF1 bit 0 : 0 = receive active high (default)  
1 = receive active low
3. MIRRX are the modulated outputs. (500k)

## Amplitude Shift Keyed IR Transmit Timing

Table 2-10. ASK IR Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Modulated output bit time				us
t2	Off bit time				us
t3	Modulated output "off"	0.8	1	1.2	us
t4	Modulated output "on"	0.8	1	1.2	us
t5	Modulated output "on"	0.8	1	1.2	us
t6	Modulated output "off"	0.8	1	1.2	us



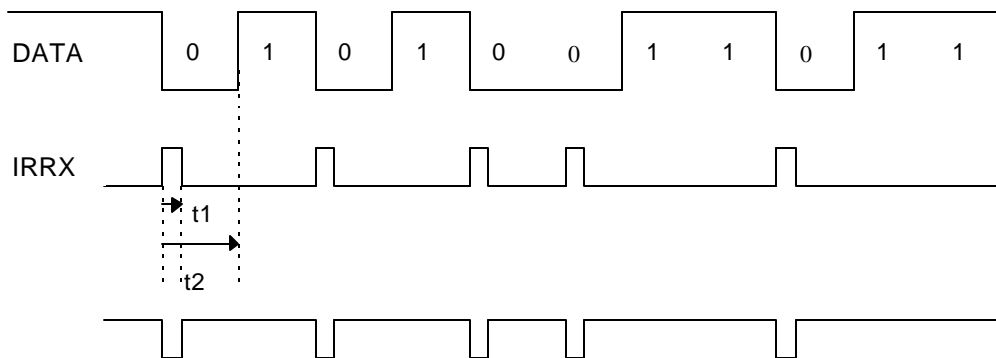
## Notes :

1. t1, t2 timing referred to IrDA Transmit Timing @ each baud rate.
2. UART1, UART2, UART3 0xF1 bit 1: 0 = receive active high (default)  
1 = receive active low
3. MIRT are the modulated outputs. (500k)

IrDA Receive Timing

Table 2-11. IrDA Receive Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Pulse width at 115k baud	1.4	1.6	2.71	us
t1	Pulse width at 57.6k baud	1.4	3.22	3.69	us
t1	Pulse width at 38.4k baud	1.4	4.8	5.53	us
t1	Pulse width at 19.2k baud	1.4	9.7	11.07	us
t1	Pulse width at 9.6k baud	1.4	19.5	22.13	us
t1	Pulse width at 4.8k baud	1.4	39	44.27	us
t1	Pulse width at 2.4k baud	1.4	78	88.55	us
t2	Bit time at 115k baud		8.68		us
t2	Bit time at 57.6k baud		17.4		us
t2	Bit time at 38.4k baud		26		us
t2	Bit time at 19.2k baud		52		us
t2	Bit time at 9.6k baud		104		us
t2	Bit time at 4.8k baud		208		us
t2	Bit time at 2.4k baud		416		us



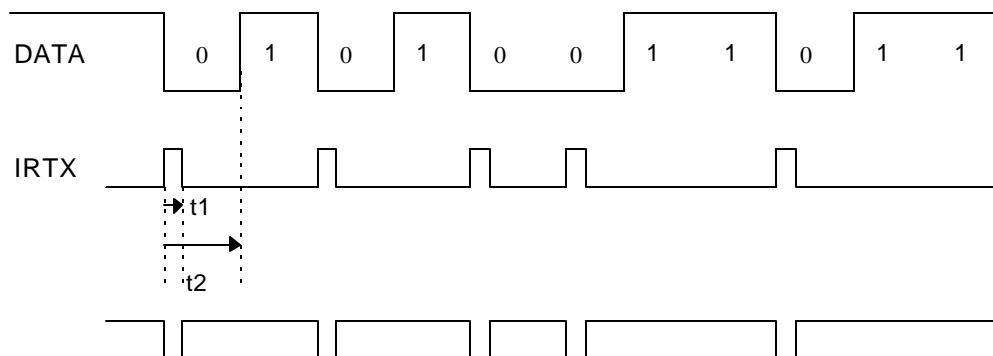
Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2, UART3 0xF1 bit 0 : 0 = receive active high (default)  
1 = receive active low

## IrDA Transmit Timing

Table 2-12. IrDA Transmit Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Pulse width at 115k baud	1.4	1.6	2.71	us
t1	Pulse width at 57.6k baud	1.4	3.22	3.69	us
t1	Pulse width at 38.4k baud	1.4	4.8	5.53	us
t1	Pulse width at 19.2k baud	1.4	9.7	11.07	us
t1	Pulse width at 9.6k baud	1.4	19.5	22.13	us
t1	Pulse width at 4.8k baud	1.4	39	44.27	us
t1	Pulse width at 2.4k baud	1.4	78	88.55	us
t2	Bit time at 115k baud		8.68		us
t2	Bit time at 57.6k baud		17.4		us
t2	Bit time at 38.4k baud		26		us
t2	Bit time at 19.2k baud		52		us
t2	Bit time at 9.6k baud		104		us
t2	Bit time at 4.8k baud		208		us
t2	Bit time at 2.4k baud		416		us



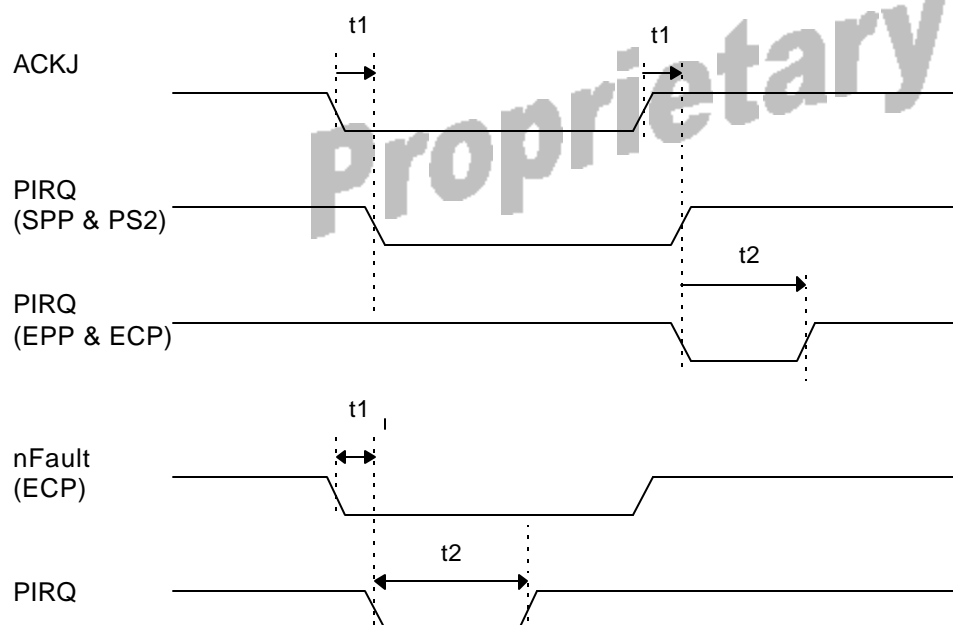
## Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. UART1, UART2, UART3 0xF1 bit 1 : 0 = transmit active high (default)  
1 = transmit active low

Parallel Port Interrupt Timing

Table 2-13. Parallel Port Interrupt Timing

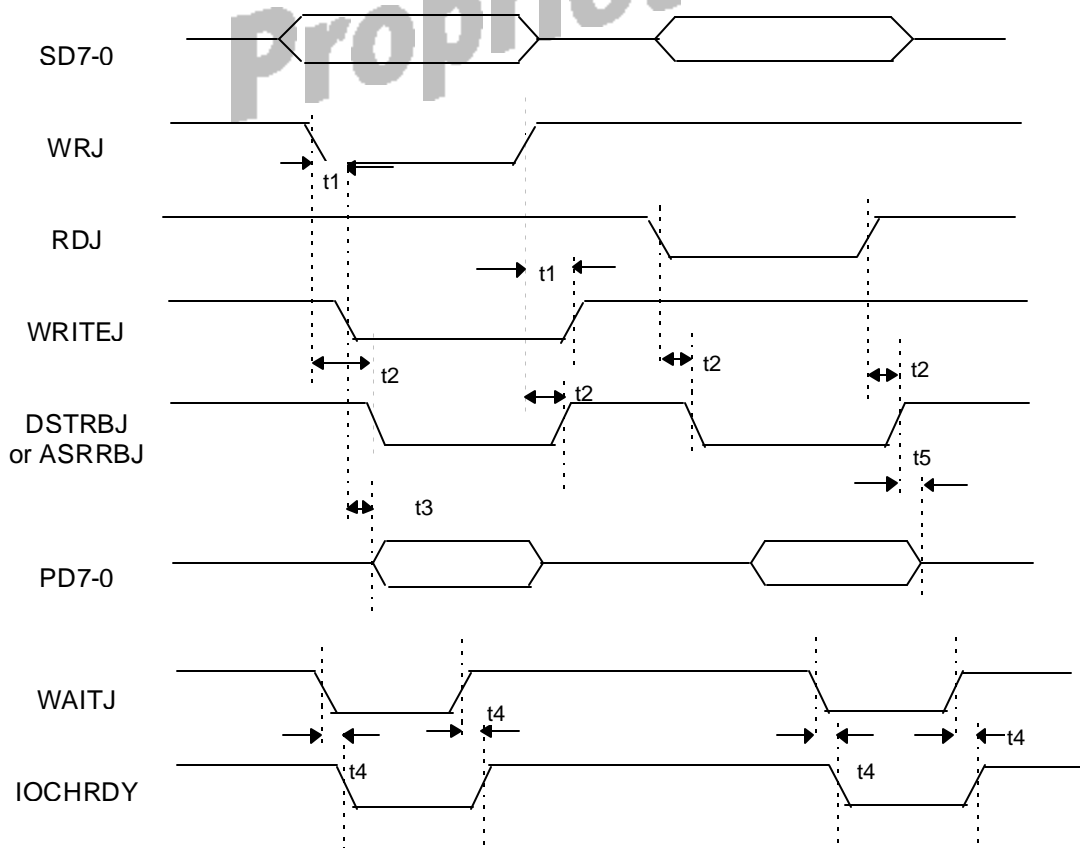
Symbol	Parameter	Min	Typ	Max	Unit
t1	PIRQ delay from ACKJ, nFault			30	ns
t2	PIRQ active in EPP & ECP modes	250		375	ns



## EPP Mode Version 1.7 Timing

Table 2-14. EPP Mode Version 1.7 Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	WRJ active to WRITEJ active			95	ns
t2	WRJ active to WRITEJ & DSTRBJ/ASTRBJ active			140	ns
t3	WRITEJ active to PD7-0 valid			40	ns
t4	WAITJ active to IOCHRDYJ active			180	ns
t5	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	90			ns

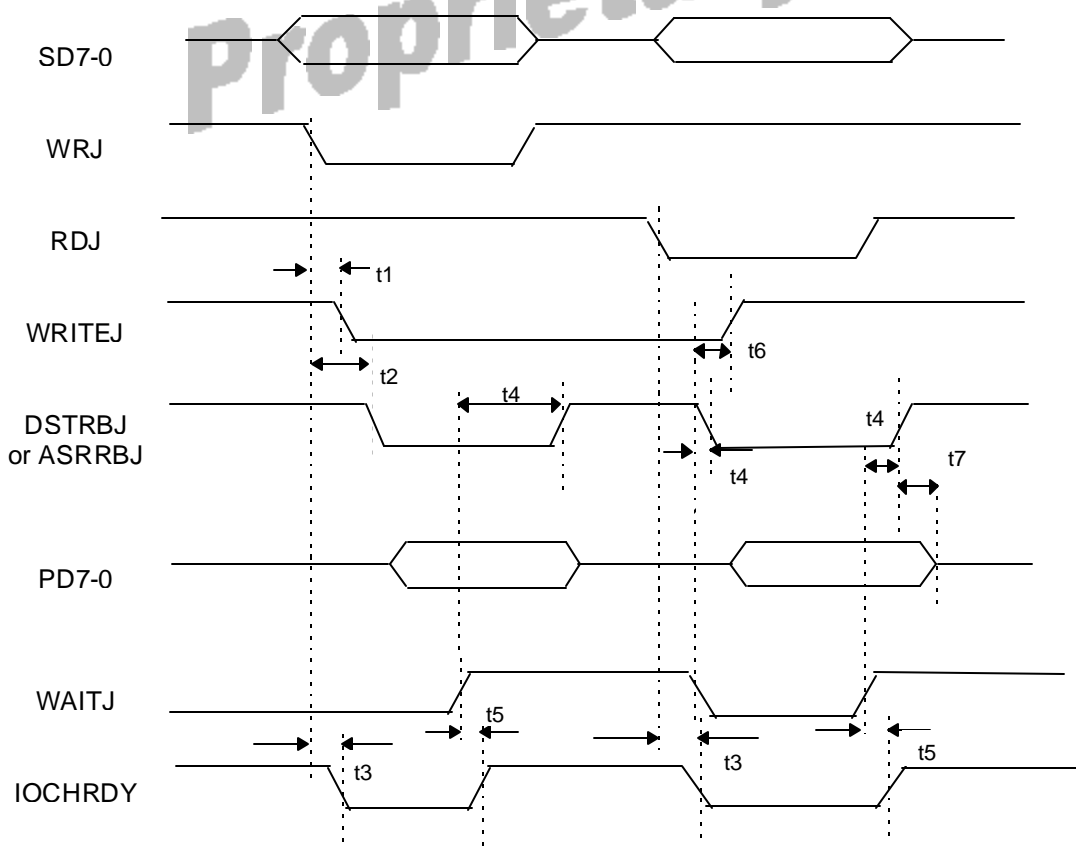




EPP Mode version 1.9 Timing

Table 2-15. EPP Mode version 1.9 Timing

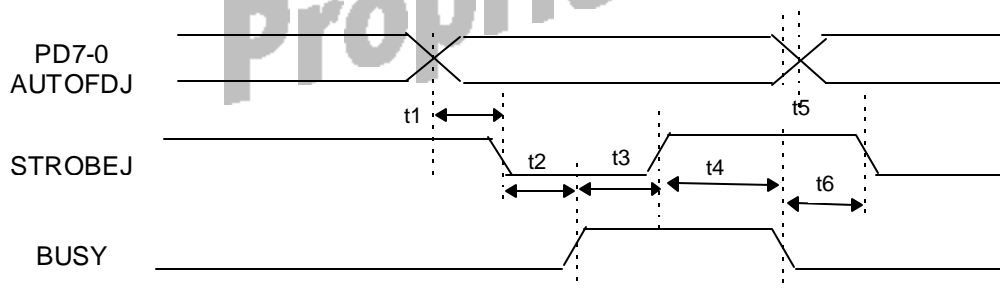
Symbol	Parameter	Min	Typ	Max	Unit
t1	WRJ active to WRITEJ active			95	ns
t2	WRJ active to DSTRBJ/ASTRBJ active			220	ns
t3	WRJ active to IOCHRDY active			180	ns
t4	WAITJ inactive to DSTRBJ/ASTRBJ inactive			700	ns
t5	WAITJ inactive to IOCHRDY inactive			180	ns
t6	WAITJ active to WRITEJ inactive			180	ns
t7	DSTRBJ/ASTRBJ inactive to PD7-0 invalid	90			ns



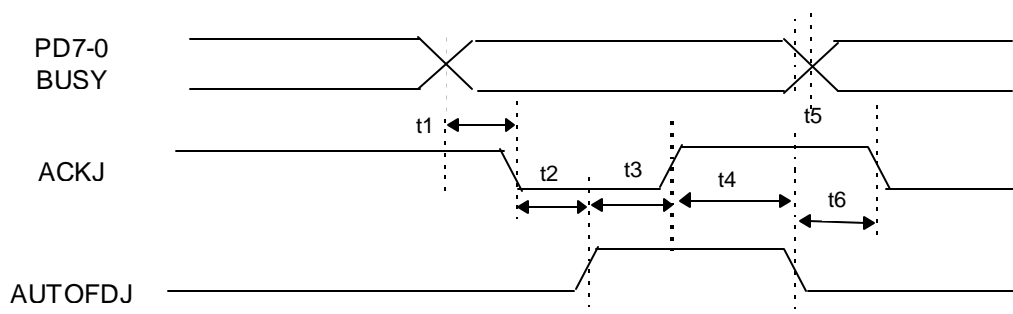
## ECP Mode Timing

Table 2-16. ECP Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	DATA valid to STROBEJ active	0			ns
t2	STROBEJ active to BUSY active	0		130	ns
t3	BUSY active to STROBEJ inactive	75			ns
t4	STROBEJ inactive to BUSY inactive	0		135	ns
t5	BUSY inactive to DATA update	0		1.1	us
t6	BUSY inactive to STROBEJ active	0			ns



ECP Forward Timing Diagram

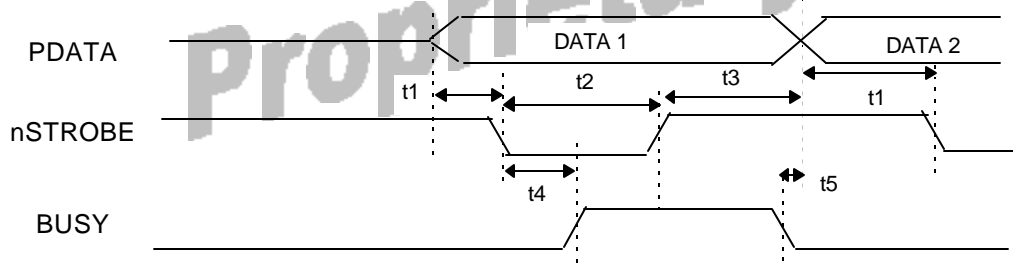


ECP Backward Timing Diagram

Compatible FIFO Mode Timing

Table 2-17. Compatible FIFO Mode Timing

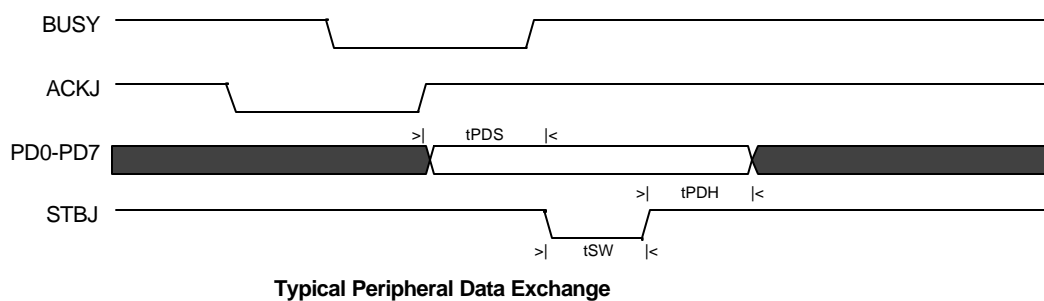
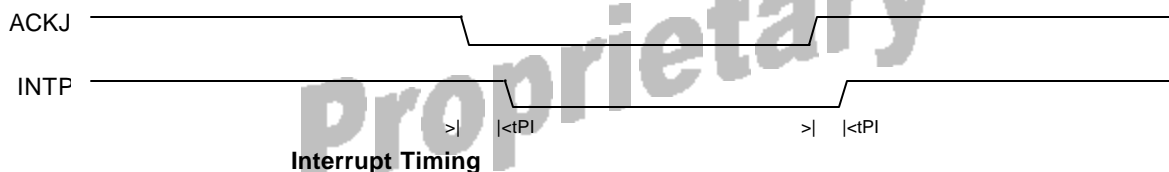
Symbol	Parameter	Min	Typ	Max	Unit
t1	Data valid to nSTROBE active		500		ns
t2	nSTROBE active pulse width		500		ns
t3	Data hold from nSTROBE inactive		500		ns
t4	nSTROBE active to BUSY active		500		ns
t5	BUSY inactive to PDATA TRANSING	80			ns



## Parallel Interface

Table 2-18. Parallel Interface

Symbol	Parameter	Min	Max	Unit
tPDH	Port Data Hold	500		ns
tPDS	Port Data Setup	500		ns
tPI	Port Interrupt	33		ns
tSW	Strobe Width	500		ns



**Section 3 : Revision History**

v.0.80 initial version

v.0.90 06/24/99

v.0.91 06/26/99

pp.4,7 have gone through correction/s 08/04/99

v.1.00 09/99

pp.4,5,7,9,12,52,53 v.1.10 12/06/99

M1535/M1535D v1.10 part 3 has merged with M1535+/M1535D+ part 3 and referred to as the South Bridge  
v.0.90 04/19/2000

V.1.00 08/24/00 (50) Printout.

**Worldwide Distributors and Sales Offices:****Taiwan****Acer Laboratories Inc. ([www.ali.com.tw](http://www.ali.com.tw))**

11F, no. 45 Tung Hsing Road,  
Taipei 110, Taiwan, R.O.C.  
Tel: +886 (2) 8768 -2800  
Fax: +886 (2) 8768 -3030

**Acer Sertek**

8F, no.88, Sec. 1  
Hsin Tai Wu Road, HsiChih,  
Taipei Hsien 221, Taiwan  
Tel: +886 (2) 2696-3232  
Fax: +886 (2) 2696- 3535

**Arrow / Ally, Inc.**

16F, 100, Sec. 1,  
Hsin Tai Wu Road, HsiChih,  
Taipei Hsien, Taiwan  
Tel: +886 (2) 2696 - 7388  
Fax: +886 (2) 2696 - 7399

**Asec International Inc.**

4F, 223 Chung Yang Road,  
Nan Kang 115, Taipei,  
Taiwan  
Tel: +886 (2) 2786-6677  
Fax: +886 (2) 2786 - 5257

**Hong Kong****Lestina International Ltd.**

[www.lestina.com](http://www.lestina.com)  
14/F, Park Tower,  
15 Austin Road, Tsimshatsui,  
Kowloon, Hong Kong  
Tel: +852-2735 -1736  
Fax: +852-2730 – 5260, 852-2730-7538

**Singapore****Ingram Micro Asia Ltd.**

205 Kallang Bahru, # 04-00,  
Singapore 339341  
Tel: +65 - 298 - 0888  
Fax: +65 - 298 - 0134

**Japan****Unidux Inc.**

1-6-4, Osaki,  
Shinagawa-Ku, Tokyo 141-8570, Japan  
Tel: +81 (3) 3779 - 7817  
Fax: +81 (3) 3779 - 7800

**Macnica, Inc.**

[www.macnica.co.jp](http://www.macnica.co.jp)  
Hakusan High-Tech Park, 1-22-2 Hakusan,  
Midori-Ku, Yokohama City 226-8505, Japan  
Tel: +81 (45) 939 - 6116  
Fax: +81 (45) 939 – 6117

**Teksel Co. Ltd.**

TBC, 2-27-10, Higashi,  
Shibuya-Ku, Tokyo 150-0011 Japan  
Tel: +81 (3) 5467-9095  
Fax: +81 (3) 5467-9346

**Korea****Acetronix Co.**

5F Namhan Bldg.,  
76-42, Hannam-Dong, Yongsan-Ku,  
Seoul 140-210, Korea  
Tel. : +82 (2) 796-4561  
Fax. : +82 (2) 796-4563

**Italy****EL.CO.MI. SRL**

Via Cassanese, 27  
20090 Segrate - (MI), Italy  
Tel: +39-2-26927430  
Fax: +39-2-26927410

**U.S.A.****ALi U. S. Office/European Operations**

[www.acerlabs.com](http://www.acerlabs.com)  
525 East Brokaw Road  
San Jose, CA 95112 USA  
Tel: +1 (408) 544 - 3100  
Fax: +1 (408) 544 - 3135

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